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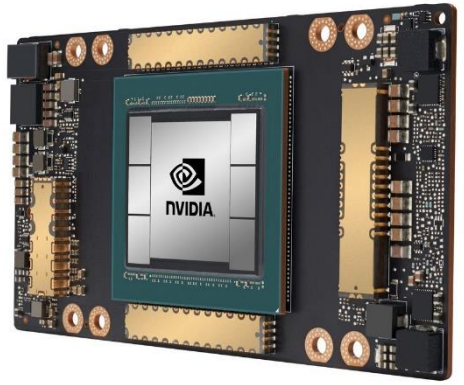

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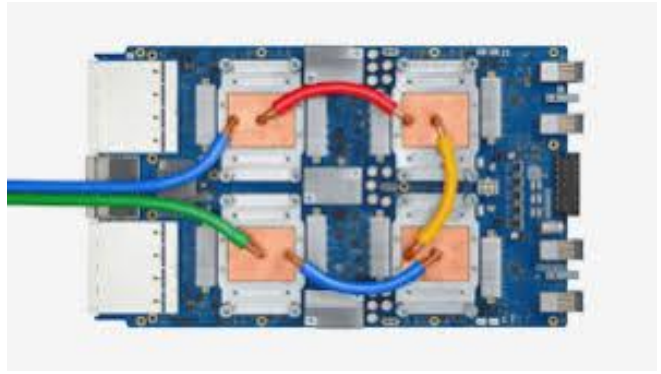


The content of this lecture is adapted from the lectures of Larry Zheng and Steve Engels

CSCB58 Week 4: Summary

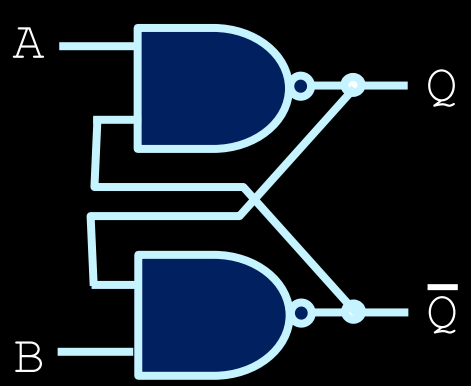
Week 4 Summary

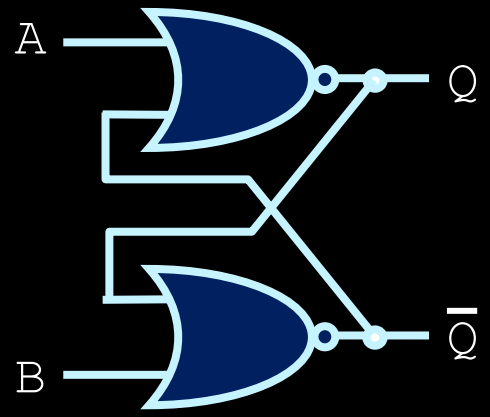
We learned

- Sequential circuits – circuits with memory
- Latches
- Flip-flops

Latches

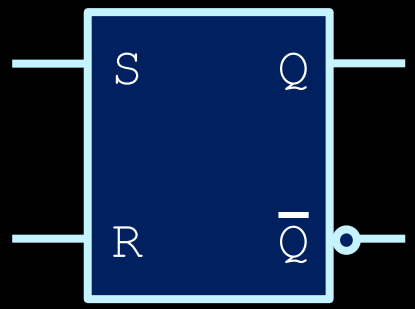
- If multiple gates of these types (NAND or NOR with feedback) are combined, you can get more steady behaviour.



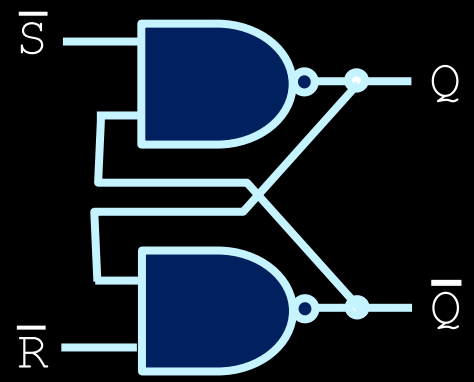


- These circuits are called latches.

S’R’ Latch



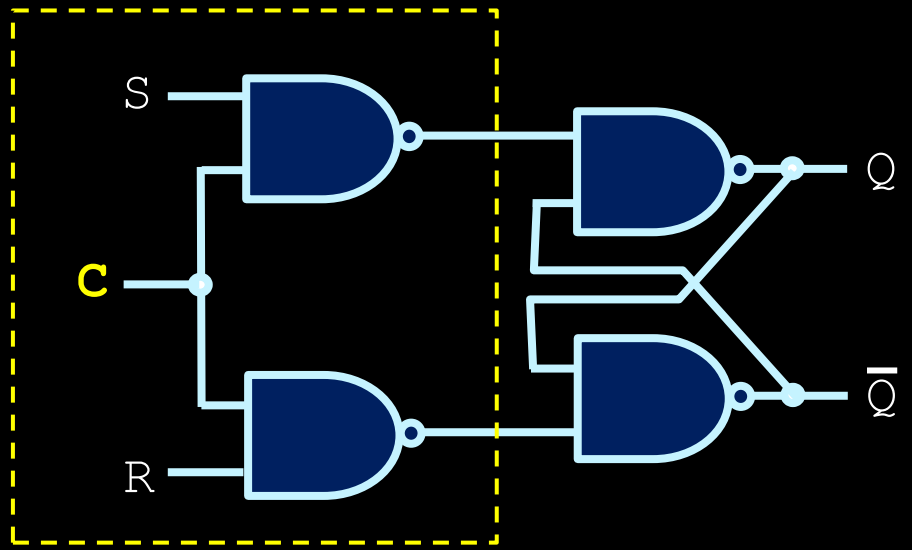
S'R' latch



$\overline{S}$	$\overline{R}$	Q_T	$\overline{Q}_T$	Q_{T+1}	$\overline{Q}_{T+1}$
0	0	X	X	1	1
0	1	X	X	1	0
1	0	X	X	0	1
1	1	0	1	0	1
1	1	1	0	1	0

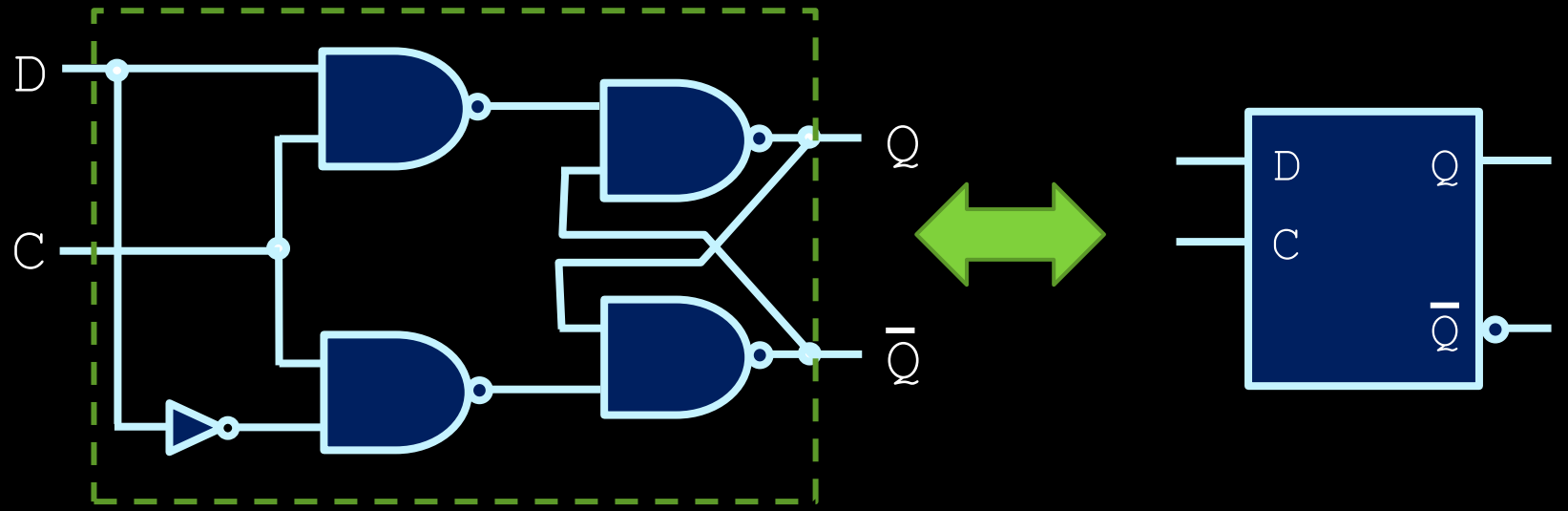
- S and R are called "set" and "reset" respectively.
- When S' = 0, R' = 1, Q is 1
- When S' = 1, R' = 0, Q is 0
- When S'R' = 11, same as previous state (01 or 10)
- How about going from oo to 11
  - Depends on whether it changes from 00 to 01 to 11, or from 00 to 10 to 11 (race condition)
  - unstable behaviour

Clocked SR latch



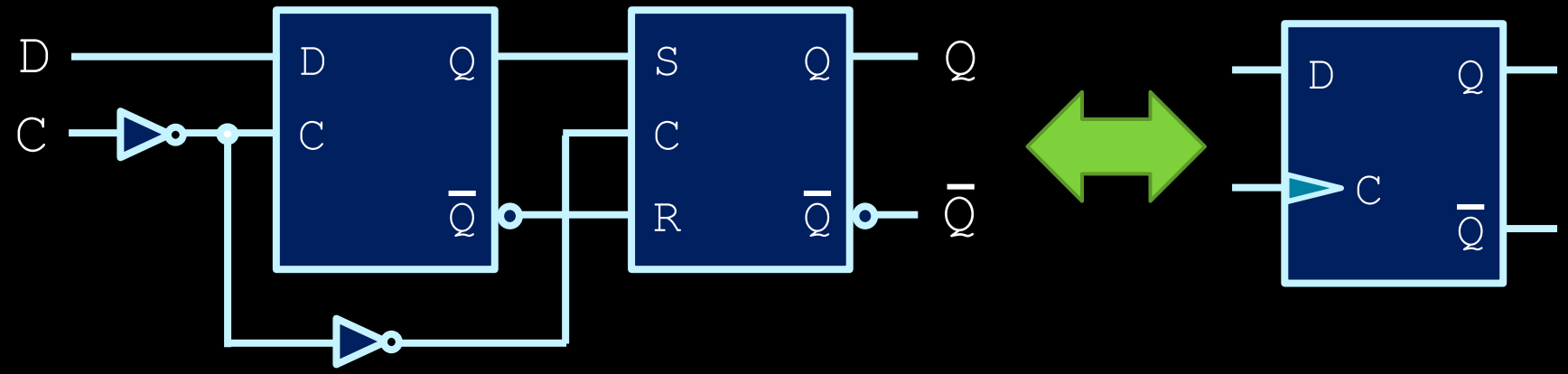
- By adding another layer of NAND gates to the $\overline{S}\overline{R}$ latch, we end up with a clocked SR latch circuit.
- The clock is often connected to a pulse signal that alternates regularly between 0 and 1.

D latch



Edge-triggered flip-flop

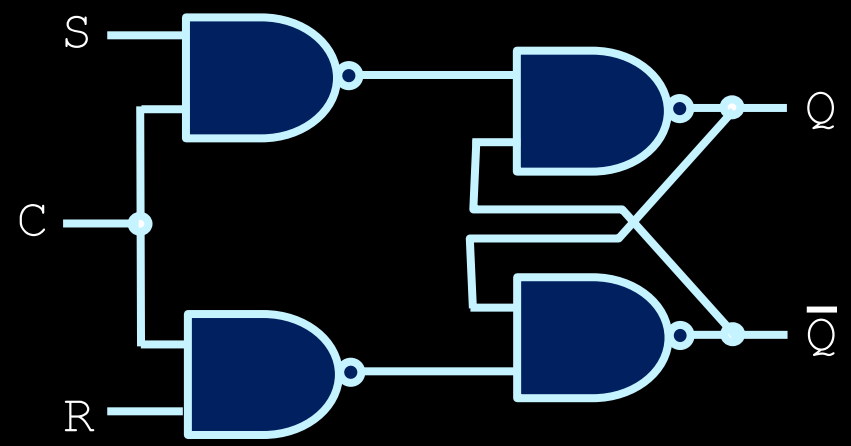
- Positive-edge triggered flip-flops



- These are the most commonly-used flip-flop circuits (and our choice for the course).

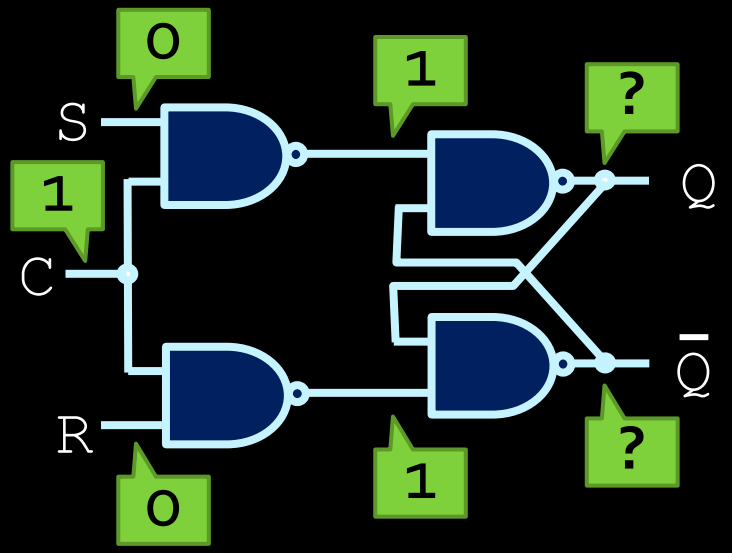
Question #1

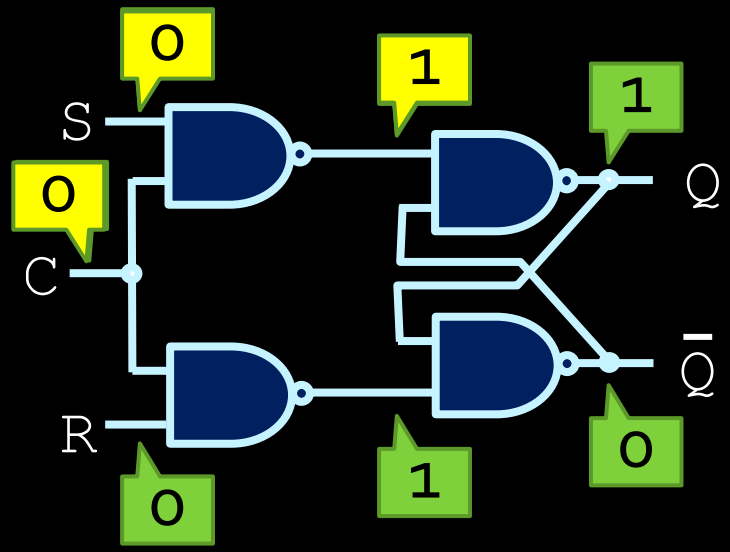
- What are the output values from Q and $\overline{Q}$ given the following inputs on S, R and C?



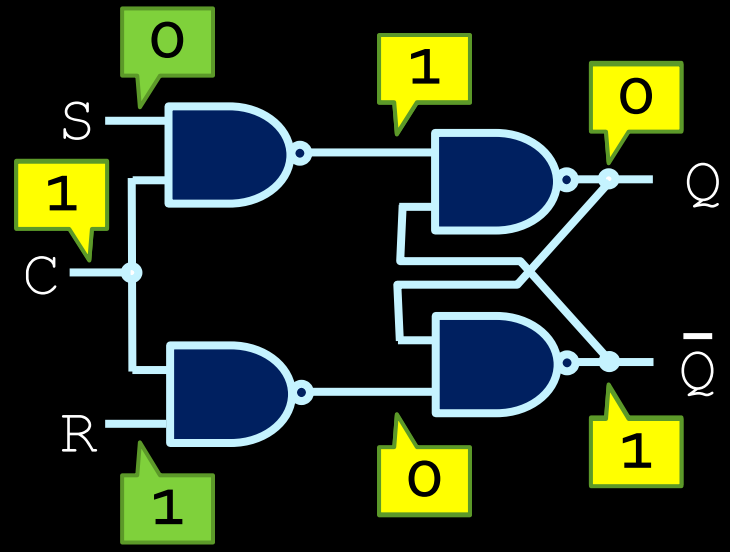
Time

S	R	C	Q	$\overline{Q}$
0	0	1		
1	0	1		
1	0	0		
0	0	0		
0	1	0		
0	1	1		



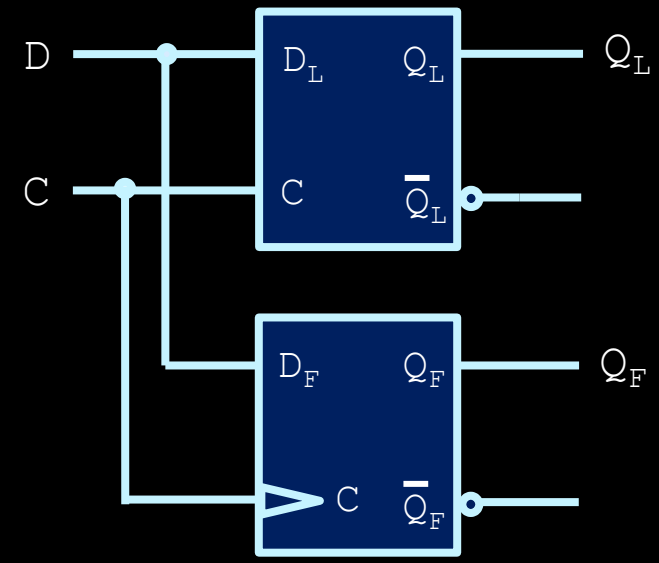


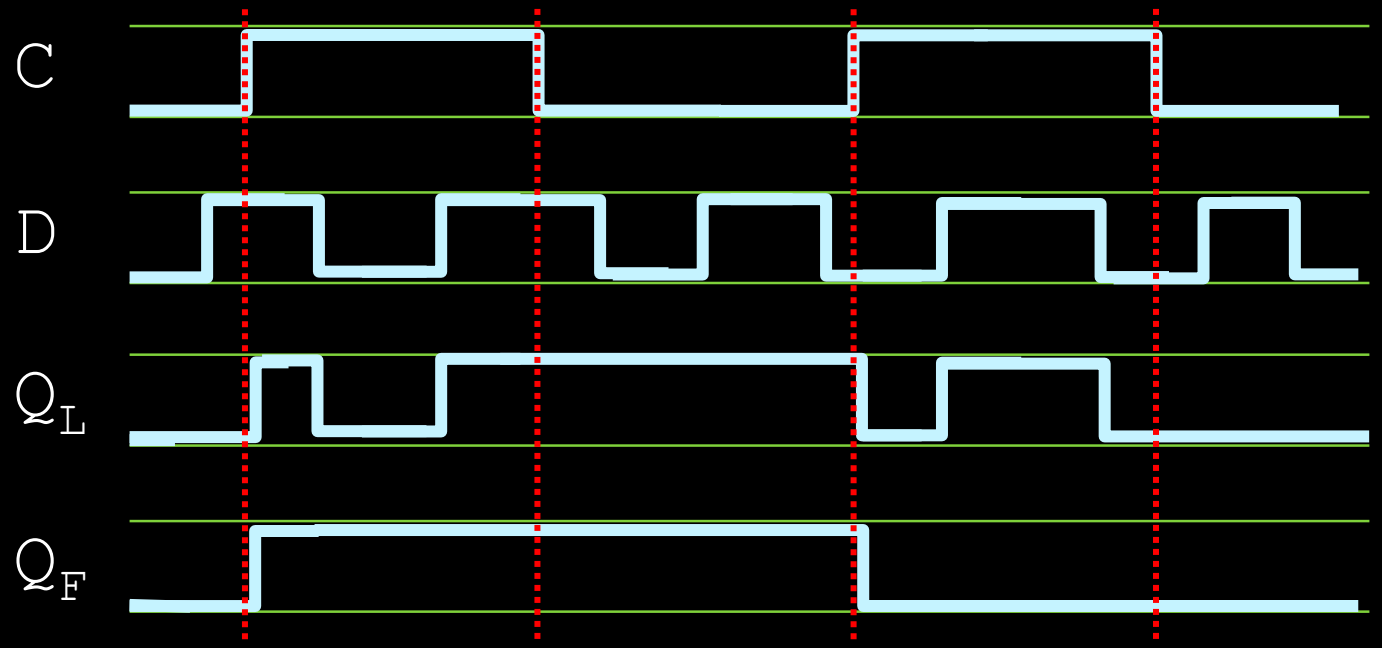
S	R	C	Q	Q̄
0	0	1		
1	0	1		
1	0	0		
0	0	0		
0	1	0		
0	1	1		



Question #2

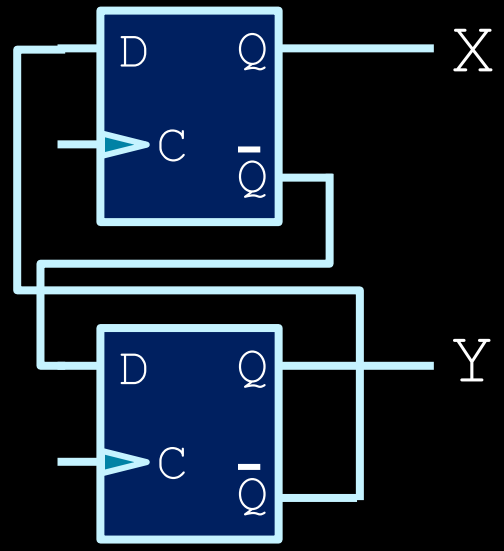
- Given the circuit on the right and the input waveform below, what will the outputs be on Q_L and Q_F?
  - What other info do you need?

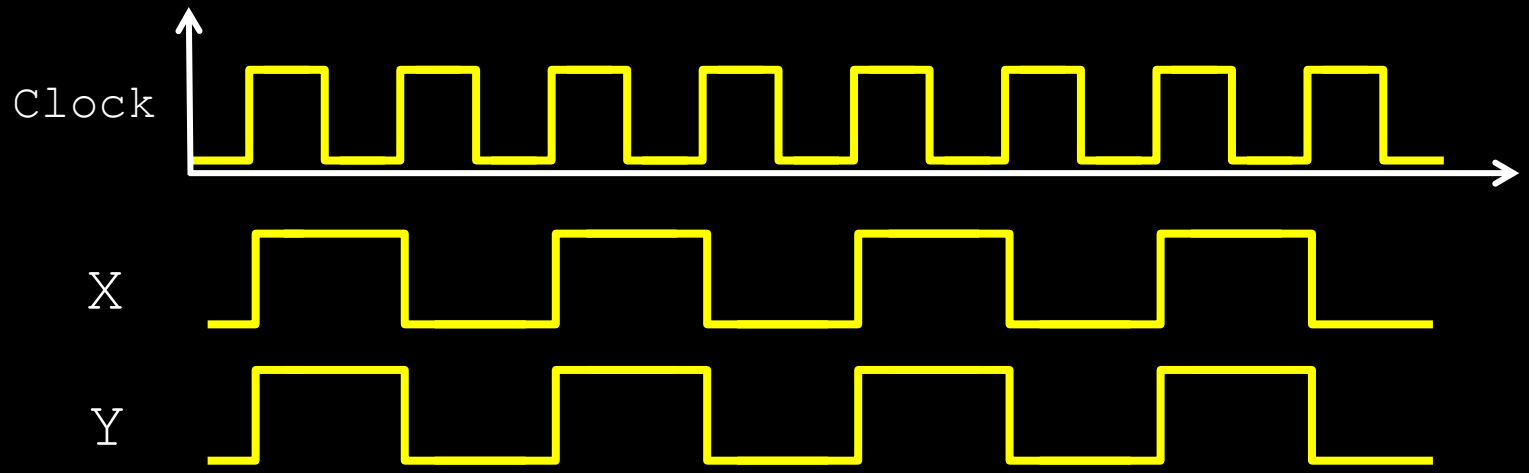




Question #3

- Assuming the Q outputs of both flip-flops start off low, what will the value of X & Y be over the next few clock cycles?
  - also assume positive edge trigger.





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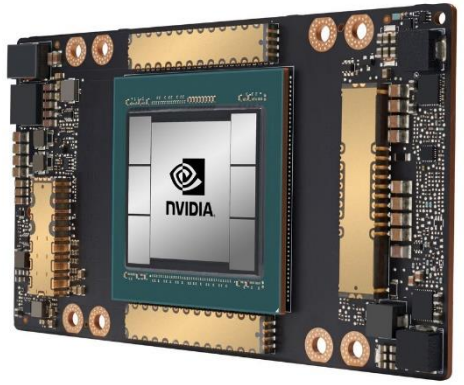

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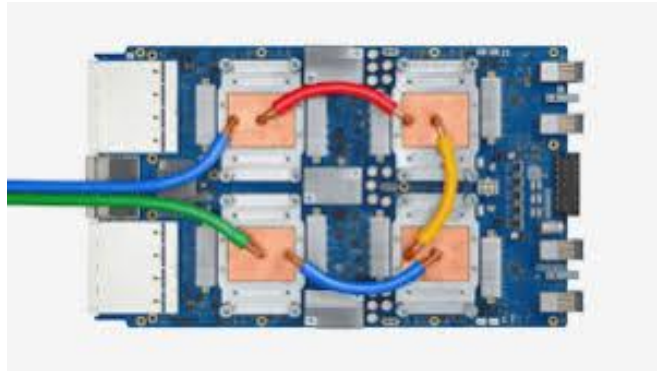

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