
HORIZONTALLY FUSED TRAINING ARRAY: AN EFFECTIVE HARDWARE UTILIZATION SQUEEZER FOR TRAINING NOVEL DEEP LEARNING MODELS

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ABSTRACT

Driven by the tremendous effort in researching novel deep learning (DL) algorithms, the training cost of developing new models increases staggeringly in recent years. We analyze GPU cluster usage statistics from a top research institute for more insights into the hardware efficiency achieved by typical DL training jobs. Our study reveals that single-accelerator training jobs can dominate the cluster-wide resource consumption when launched repetitively (e.g., for hyper-parameter tuning) while severely under-utilizing the hardware. Fortunately, we observe that such workloads have the following unique characteristics: (i) the models among jobs often have the same types of operators with the same shapes, and (ii) the inter-model horizontal fusion of such operators is mathematically equivalent to other already well-optimized operators. Thus, to help DL researchers and practitioners effectively improve the hardware utilization of their novel DL training workloads, we propose **Horizontally Fused Training Array (HFTA)**. HFTA is a new DL framework extension library that *horizontally fuses* the models from different repetitive jobs deeply down to operators and then trains them simultaneously on a shared accelerator. To show the generality of our solution, we apply HFTA to six DL models training on state-of-the-art accelerators (GPUs and TPUs). Our results indicate that HFTA is highly effective in improving hardware utilization and achieves up to $15.1\times$ higher training throughput vs. the standard practice of running each job on a separate accelerator.

1 INTRODUCTION

Deep Learning (DL) algorithms have facilitated tremendous progress in a range of domains, including natural language translation (Wu et al., 2016), recommendation systems (Nau-mov et al., 2019), magnetic resonance imaging segmentation (Akkus et al., 2017), video game bots (OpenAI, 2018), real-time high-resolution rendering (NVIDIA, 2020e), and very-large-scale integrated circuit placement (Lin et al., 2019). This is driven by the abundant and continuous efforts in researching and developing novel DL models by academia and industry in recent years. Developing these models is computationally intensive, requiring an army of expensive, specialized accelerators such as GPUs and TPUs (Jouppi et al., 2017), leading to staggeringly high training costs (Coleman et al., 2017; Amodei et al., 2018; Zhu et al., 2018; Mattson et al., 2020; Zhu et al., 2020).

To reduce this training cost and optimize the cluster-wide hardware resource usage, we analyze GPU usage statistics over two consecutive months on a large GPU cluster from the Vector Institute (Vector Institute, 2021). We observe that, despite significant attention on optimizing DL train-

ing workloads from the computer system and architecture communities, especially on distributed training optimizations (Appleyard et al., 2016; Chen et al., 2016; Lin et al., 2018; Rajbhandari et al., 2019; Mattson et al., 2020), single-accelerator (e.g., single-GPU) training jobs, often launched repetitively by DL researchers (to perform *hyper-parameter tuning*, *model architecture search* or *convergence stability tests*), can (i) dominate the cluster-wide hardware resource consumption (e.g., 46.2% in our study) while (ii) having extremely low hardware utilization (Section 2.1 and 5.3).

The root cause of this phenomenon is manifold. DL researchers and practitioners often lack the expertise to optimize their training workloads independently. As a result, basic techniques, such as increasing the batch size, often become the only approach at their disposal to improve hardware utilization. However, this technique can be impractical due to many reasons, including generalization gap (Keskar et al., 2017), batch size scaling limit (Shallue et al., 2019), and GAN training instability (Odena, 2019). On the other hand, accelerators (e.g., GPUs and TPUs) evolve towards more computing power and larger memory capacities (Table 2 and 3). This trend amplifies the severity of the hardware under-utilization caused by the inability of such training workloads to scale their performance well.

Thus, this phenomenon motivates *hardware sharing* approaches. To the best of our knowledge, the only widely used hardware-based sharing solutions applicable to DL

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training are the MPS (NVIDIA, 2020h) and MIG (NVIDIA, 2020g) features on NVIDIA GPUs. However, as we later show in Section 2.2, these generic GPU sharing features that aim at arbitrary workloads are far from the “silver bullets” to effectively improve the hardware utilization in the case of repetitive single-GPU training workloads. The situation is even worse for emerging DL accelerators (e.g., TPUs) that currently do not have any hardware-based sharing features.

To address such hardware under-utilization on various accelerators, we make two key observations based on the unique characteristics of these workloads. First, the models across jobs belonging to the same workload (e.g., hyper-parameter tuning) often have the *same types* of operators with the *same shapes*. Second, if these operators are horizontally fused across the models, the outcome is mathematically equivalent to other well-optimized operators found in existing DL framework stacks and accelerators (e.g., fusing multiple convolution operators can be realized using grouped convolutions). Inspired by these key observations, we propose to horizontally merge multiple training jobs with the same or similar DL models by deeply *fusing* most, if not all, operators in those models. These models’ training is then performed collectively on the same shared accelerator (instead of training each model separately on its accelerator). Our proposed idea of *inter-model horizontal fusion* is drastically different from and also more effective than major-related prior works as it better exercises the full potential of modern accelerators while (i) not relying on the generic sharing primitives (e.g., CUDA streams) that are ineffective for repetitive single-GPU workloads, and (ii) avoiding limited fusion techniques that, for example, support only stateless operators or require the weights across models to be the same (Narayanan et al., 2018a).

We leverage this novel idea to build a new DL framework extension library for DL researchers and practitioners, called **Horizontally Fused Training Array (HFTA)**¹, that significantly simplifies the adoption of our proposed inter-model horizontal fusion technique. In summary, this work makes the following major contributions.

- To understand the nature of the jobs running on modern DL accelerator clusters, we collect and study GPU cluster usage statistics, including 51K jobs running for 472K GPU hours in total, from real research workloads. The results of this study demonstrate that repetitive single-accelerator training jobs (i) dominate the hardware resource usage (i.e., 46.2%) and (ii) have extremely low hardware utilization.
- Motivated by this study, we make two key observations about these jobs that our proposal is built upon: (1) The models often have the same types of operators with the same shapes. (2) The inter-model horizontal fusion of such

operators is mathematically equivalent to other existing and well-optimized operators.

- We develop HFTA, a new library that helps DL researchers and practitioners (even with a limited computer system and architecture expertise) to easily extract better performance from their hardware when training novel DL models. While doing so, we avoid (i) introducing any additional device-specific operator implementations that would limit the generality of our idea across different accelerators and (ii) any effect on individual models’ convergence as the speedup is achieved only through mathematically equivalent transformations. HFTA applies to a wide variety of models and can run on any hardware backends supported by existing DL frameworks. Furthermore, we propose a simple yet effective method to integrate HFTA into existing tuning algorithms and develop a lightweight tuning framework named **Horizontally Fused Hyper-parameter Tuning (HFHT)**.

- We evaluate HFTA on six highly impactful DL models, covering a wide range of tasks, in the machine learning (ML) community. On modern GPUs (V100, RTX6000 and A100), HFTA achieves $2.42\times$ to $11.50\times$ higher training throughput than running the training jobs without sharing, which is commonly employed by hyper-parameter tuning frameworks (Li, 2020), $1.25\times$ to $4.72\times$ than MPS and $1.33\times$ to $4.88\times$ than MIG. HFTA can also fit $1.50\times$ to $9.43\times$ more training jobs on the same GPU than MPS. On TPUs, HFTA achieves $2.98\times$ to $15.13\times$ higher training throughput, which demonstrates HFTA’s ability to improve performance across different hardware backends significantly. Finally, when HFTA is integrated into two tuning algorithms via HFHT, we reduce the cost of total GPU hours by up to $5.10\times$ among four end-to-end hyper-parameter tuning workloads.

2 BACKGROUND AND MOTIVATION

2.1 Inefficiency in Repetitive Training Jobs

As DL research continues to evolve in recent years, the accompanied training cost increased dramatically. For example, (Amodei et al., 2018) show that the amount of compute for training SOTA DL models doubles every 3.4 month, outpacing even Moore’s Law (Schaller, 1997). Motivated by the practical goal of reducing cluster-wide training cost, using the methodology detailed in Appendix A, we collect and study the GPU usage statistics of real research workloads for two consecutive months on a large GPU cluster from the Vector Institute (Vector Institute, 2021). To our surprise, we find that single-accelerator (e.g., single-GPU) training jobs dominate the cluster-wide hardware resource consumption when these jobs are launched repetitively in groups, and the aggregated cost of these jobs can even outweigh that of distributed training (the primary focus of many research efforts from the computer system and architecture communities (Lin et al., 2018; Jayarajan et al., 2019; Rajbhandari et al., 2019; Mattson et al., 2020; Li et al., 2020)).

¹<https://github.com/UofT-EcoSystem/hfta>

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Table 1. GPU hour usage breakdown for two consecutive months of a large GPU cluster from the Vector Institute.

Training Jobs	Repetitive Single-GPU	Isolated Single-GPU	Distributed	Other
GPU Hours	218K(46.2%)	19K(3.5%)	113K(24.0%)	124K(26.3%)

Potential reasons of these repetitive jobs include (but are not limited to) hyper-parameter tuning (Strubell et al., 2019) and convergence stability testing.

Background *Hyper-parameter tuning* finds the optimal set of hyper-parameters unknown a priori, which are usually necessary for building accurate models targeting a previously unexplored problem (Bergstra et al., 2011; Bergstra & Bengio, 2012). Typical hyper-parameters include learning rates, the choices of weight initializers, and optimizer settings. *Model architecture search* (Elsken et al., 2019) is a subset of hyper-parameter tuning where the hyper-parameters directly impact the model architecture (e.g., the number of layers). *Convergence stability testing* trains the same model many times with different random seeds to verify the final accuracy results.

In our study, we classify the jobs into four main categories: (1) multi-node or single-node distributed training, (2) repetitive single-GPU training, (3) isolated single-GPU training, and (4) others (meaning the jobs that do not belong to the first three categories or can not be identified). Table 1 shows the GPU hour usage distribution among these categories, from which we can observe that the repetitive single-GPU training jobs consume as much as 46.2% of the cluster-wide total GPU hours. Furthermore, those repetitive single-accelerator training jobs often have low hardware utilization, as we show in Appendix A. The cause of such phenomenon is manifold:

- Improving the hardware utilization for DL training jobs can be very challenging. DL researchers and practitioners often lack the system and architecture expertise to optimize their training workloads independently. Increasing the batch size, which is the naïve and often the only approach at their disposal to increase hardware utilization, is not universally applicable. For instance, large batch sizes can lead to training instability for the generative adversarial networks (GAN) (Odena, 2019; Brock et al., 2019), generalization gap (Keskar et al., 2017), and diminishing returns due to batch size scaling limit (Shallue et al., 2019). Even with the help from the computer system and architecture experts, applying various advanced optimization techniques (e.g., kernel fusion (Appleyard et al., 2016) or checkpointing (Chen et al., 2016; Zheng et al., 2020)) on each new model requires an enormous amount of engineering efforts (Mattson et al., 2020). Meanwhile, novel DL models are being proposed at the exponential pace in recent years (Charrez, 2019).

- As DL research progresses, accelerators (e.g., GPUs and TPUs (Jouppi et al., 2017)) evolve towards more compute

Table 2. Cloud TPU Core Specifications (Google, 2020c)

TPU	v2 (2017)	v3 (2018)	v4 (2020) [†]
MXUs	1	2	≥ 4 ?
Memory (HBM)	8 GB	16 GB	? GB

[†] TPU v4 is expected to double the FLOPs of TPU v3 along with other enhancements (Kumar, 2020).

Table 3. NVIDIA Data Center GPU Specifications

GPU	SMs	HBM (GB)	HBM Bandwidth	TC Types
P100 (2016)	56	12/16	549/732 GB/s	-
V100 (2018)	80	16/32	900 GB/s	FP16
A100 (2020)	108	40	1.6 TB/s	TF32 & FP16

power (e.g., more streaming multiprocessors (SMs) and the introduction of specialized compute units for fast matrix multiplications in GPUs called tensor cores (TCs) (Markidis et al., 2018)) and larger memory capacity/bandwidth. We can observe this trend from Tables 2 and 3 that list the specifications of the most recent NVIDIA data center GPUs and Google Cloud TPUs, where the largest accelerators suffer from under-utilization the most.

The fast development of both new DL models and accelerators together exacerbates the hardware under-utilization from repetitive single-accelerator training jobs, which motivates hardware sharing methods discussed below.

2.2 Hardware-based Sharing

The most well-known and (to the best of our knowledge) the only widely-used hardware-based sharing solutions applicable to DL training workloads² are the Multi-Process Service (MPS) (NVIDIA, 2020h) and Multi-Instance GPU (MIG) (NVIDIA, 2020g) on NVIDIA GPUs. MPS allows CUDA kernels from different processes to potentially run concurrently on the same GPU via a hardware feature called Hyper-Q (Bradley, 2007). MIG, which is currently only available on the most recent A100 GPUs (NVIDIA, 2020a), partitions a single GPU into multiple (up to 7) isolated GPU instances (GIs) where each job now run on a single GI.

However, as we quantitatively demonstrate in Section 5.1, both MPS and MIG still leave the significant potential of training performance unharnessed due to the following reasons. First, both MPS and MIG duplicate the runtime overhead among kernels from different training jobs, including kernel launches (Lustig & Martonosi, 2013), GEMM setups and teardowns (NVIDIA, 2020j), and/or memory format conversions (related explicitly to TCs) (NVIDIA, 2020f). Thus, they can not effectively improve the SM and TC utilization. Second, both MPS and MIG require running training jobs as separate processes, which duplicates the GPU memory overhead reserved by the DL framework stack (Gross et al., 2019) and leads to a higher overall GPU memory footprint. Therefore, we can fit fewer training jobs into the same GPU. Finally, MIG’s partitioning granularity can be too coarse for many training workloads. Even

²AMD GPUs also have a hardware-based sharing feature called CU-mask (Otterness & Anderson, 2020); however, we skip its discussion due to their irrelevance in mainstream training workloads.

with the finest granularity of MIG (7 GIs), each job can still under-utilize a single GI, as we show in Section 5.1.

3 OUR PROPOSAL: HFTA

To address the challenge of improving hardware utilization for novel repetitive training workloads on a variety of accelerators, we make the following two key observations on the unique characteristics of these workloads:

- When launched repetitively (such as during hyper-parameter tuning or convergence stability testing), the models used across these jobs often have the *same types* of operators with the *same shapes*.
- *Horizontally fusing* the same types of operators with the same shapes often results in other mathematically equivalent operators that already exist in many SOTA DL models and thus have been optimized in most DL framework stacks on different accelerators.

Figure 1 explains the above observations with a concrete example of hyper-parameter tuning where the goal is to determine which weight initializer and learning rate work the best. Regardless of which weight initializer or learning rate is used, the first operators in both models are Conv2d of the same shape; the horizontal fusion of many Conv2d operators is mathematically equivalent to a grouped Conv2d which is already used in the ResNeXt (Xie et al., 2017) and MobileNets (Howard et al., 2017) models and supported by cuDNN (NVIDIA, 2020c) on NVIDIA GPUs and XLA (Google, 2020e) on TPUs.

Inspired by the above observations, instead of the common practice (Li, 2020) of running each job with a single model on a separate accelerator, we propose to better utilize existing hardware by deeply fusing the the same (class of) models across multiple jobs together. Most, if not all, operators of these models can be *horizontally fused*, and we train these models simultaneously on the same accelerator. Thus, as depicted in Figure 1, we can fuse many training jobs into a single one, without the need to implement any new device-specific operator from scratch, which is both time-consuming and error-prone. Moreover, this approach easily generalizes to any hardware backends that the DL frameworks already support (e.g., all NVIDIA GPUs and Google TPUs in the case of PyTorch) Since horizontal operator fusion can be performed for both single-accelerator and distributed training, our approach applies to both use cases.

However, manually implementing or porting existing training workloads to the fused ones from scratch can be challenging for DL researchers and practitioners. To much simplify the associated engineering efforts, we develop a new DL framework library called **H**orizontally **F**used **T**raining **A**rray (**HFTA**). Even though we choose PyTorch (Paszke et al., 2019) as our prototyping DL framework due to its user-friendliness and increased popularity within the ML commu-

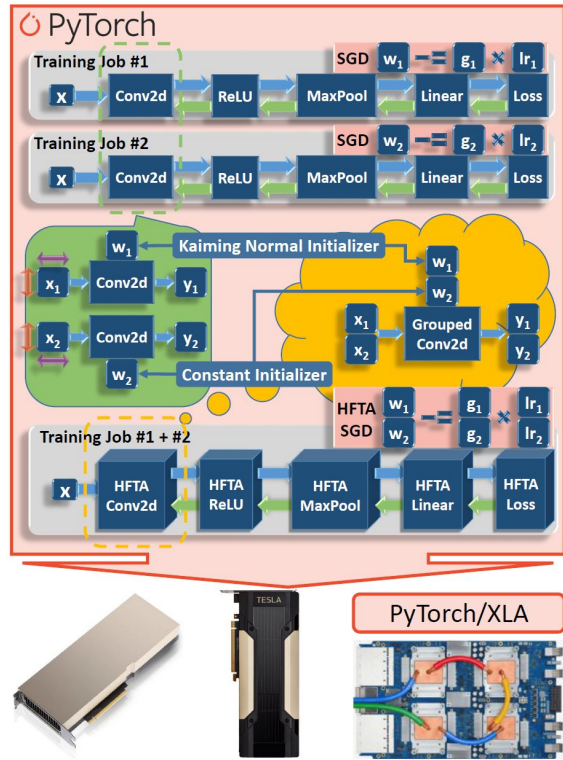


Figure 1. An example showing the key idea of HFTA where two training jobs for hyper-parameter tuning are fused into one via inter-model horizontal operator fusion.

```

B = len(args.lrs) # Number of fused training jobs.
nn.Conv2d = get_hfta_op_for(nn.Conv2d, B=B)
nn.ReLU = get_hfta_op_for(nn.ReLU, B=B)
nn.MaxPool2d = get_hfta_op_for(nn.MaxPool2d, B=B)
nn.Dropout = get_hfta_op_for(nn.Dropout, B=B)
nn.Linear = get_hfta_op_for(nn.Linear, B=B)
# Model definition.
class AlexNet(nn.Module):
    def __init__(self, ...):
        super(AlexNet, self).__init__()
        self.features = nn.Sequential(
            nn.Conv2d(...), nn.ReLU(...), nn.MaxPool2d(...),
            ...)
        self.classifier = nn.Sequential(
            nn.Dropout(...), nn.Linear(...), nn.ReLU(...),
            ...)
    
```

Figure 2. How to enable HFTA for AlexNet.

nity (He, 2019), the same idea can be implemented on top of other DL frameworks (e.g., TensorFlow (Abadi et al., 2016) and MXNet (Chen et al., 2015)). Also, HFTA is carefully designed to accommodate computer system and architecture “novices”. It can be used seamlessly with PyTorch-native training scripts and only requires changing very few lines of code. As an illustrative example, Figure 2 shows how to enable HFTA for AlexNet (Krizhevsky et al., 2012). We can observe that the model definition is kept the same with only a few extra lines of code (highlighted in the red box) to update the PyTorch’s operator classes.

We now discuss the HFTA’s individual components:

HFTA Operators To relieve the DL researchers and practitioners from the need to implement any horizontally fused operators themselves, HFTA covers most common opera-

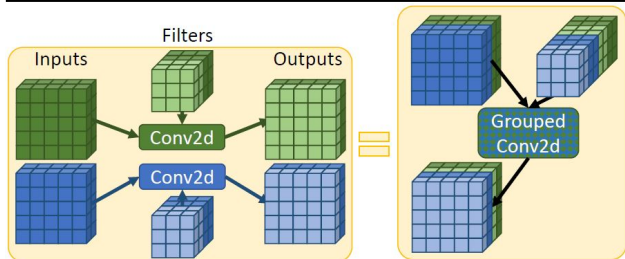


Figure 3. An example showing how two Conv2d operators can be fused into a single grouped Conv2d with two groups.

tors used in DL research and development (with detailed fusion rules provided in Appendix B). As an example, Figure 3 illustrates that the fusion of operators from the (de)convolution family (e.g., Conv2d or ConvTranspose1d) is equivalent to their grouped (de)convolution counterparts by concatenating (1) the inputs along the channel dimension, and (2) weights (filters) and biases along the dimension of the output channel.

HFTA Optimizers and Learning Rate Schedulers In addition, HFTA supports inter-model horizontally fused optimizers (e.g., Adam (Kingma & Ba, 2015) and Adadelta (Zeiler, 2012)) and learning rate schedulers (e.g., StepLR (Senior et al., 2013)). This is because (1) hyper-parameter tuning is a common use case in repetitive training workloads, and (2) learning rates, learning rate schedules, and optimizer settings (e.g., momentum (Qian, 1999; Sutskever et al., 2013)) are common hyper-parameters that require tuning for many DL models. The scalar-vector operations (e.g., multiplying a learning rate under tuning with the gradients) in the original implementations are now replaced by broadcasted vector-vector operations (e.g., multiplying a vector of learning rates with the concatenated gradients of all models) in HFTA’s implementations (as we show in Figure 1). We also plan to continue improving the HFTA’s coverage to support more operators, optimizers, and learning rate schedulers beyond this work’s publication¹.

Loss Scaling The loss functions across multiple models can be fused as well. If the loss is reduced by averaging over the mini-batch, we scale the fused loss value by the number of models under fusion to reconstruct mathematically equivalent gradients. If the loss is not reduced or reduced by sum, such scaling rule is no longer needed. We provide detailed derivations in Appendix C.

Convergence Since the fusion of all components are achieved through mathematically equivalent transformations, HFTA theoretically does not have any effect on the models’ original convergence. We also provide the related empirical validation in Appendix D.

Integration with Tuning Algorithms During hyper-parameter tuning, as a tuning algorithm proposes different sets of hyper-parameters to try, we can leverage HFTA to improve the overall hardware utilization by partitioning these sets and fusing each partition as a single training job.

To prototype this idea, we develop a lightweight hyper-parameter tuning framework called **Horizontally Fused Hyper-parameter Tuning (HFHT)**. HFHT currently supports (1) two hyper-parameter tuning algorithms (Hyperband (Li et al., 2018) and random search (Bergstra & Bengio, 2012)), and (2) not only sharing accelerators via HFTA but also sharing GPUs via MPS³ (to compare with HFTA). We discuss HFHT’s detailed design in Appendix E.

4 METHODOLOGY

Workloads Our major benchmarks are carefully selected based on the following three criteria. First, our workloads should represent important models in their corresponding DL sub-fields, making sure that HFTA is effective in improving the hardware utilization for important DL models. Second, we select models that have not yet received much attention from the computer system and architecture communities and are not over-optimized. This is a much more realistic scenario for DL researchers and practitioners who typically lack the expertise to apply advanced optimization techniques. Third, we would like to cover both compute-bound and memory-bound DL models. Based on the aforementioned criteria, two classes of models (three different workloads) are selected as our major benchmarks.

PointNet (Qi et al., 2017) is a memory-bound neural network that performs (i) object classification and (ii) segmentation tasks on 3D point clouds. The models for both tasks are trained on the ShapeNet part dataset (Yi et al., 2016). We leverage a third-party PyTorch implementation of PointNet (Xia, 2019) endorsed by Qi et al. (Qi, 2017).

DCGAN (Radford et al., 2016) is a compute-bound generative adversarial network (GAN) that synthesizes natural-apparent images. The model is trained on the LSUN dataset (Yu et al., 2015). We leverage an implementation of DCGAN from PyTorch official examples (PyTorch, 2020).

To emulate the hardware usage habits of DL researchers and practitioners without the influence from the computer system and architecture experts, the batch sizes used in both benchmarks are kept the same as reported in their corresponding publications.

To empirically validate that HFTA does not affect convergence and to demonstrate that HFTA can also improve the hardware utilization for conventional models, we further include ResNet-18 (He et al., 2016), MobileNetV3-Large (Howard et al., 2019), Transformer (Vaswani et al., 2017), and BERT-Medium (Turc et al., 2019) as our secondary benchmarks. To evaluate HFHT, for each of the the PointNet and MobileNet classification tasks, we prepare two end-to-end hyper-parameter tuning workloads using different tuning algorithms (random search and Hyperband) as

³HFHT also supports MIG. HFHT’s evaluation on MIG is not included due to space constraints.

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Table 4. Specifications of our experiment platforms. *Dev. Mem.* and *VM/Host Mem.* stands for device memory and VM/host memory respectively in GB. *CSP* stands for cloud service provider.

Accelerator	Dev. Mem.	CSP	VM Instance	CUDA	cuDNN	GPU Driver	PyTorch	PyTorch/XLA	(v)CPUs	VM/Host Mem.
V100	16	AWS	p3.2xlarge	10.2	7.6.5	450.51.05	1.6.0	-	8	61
RTX6000	24	-	-	10.2	7.6.5	450.66	1.6.0	-	8	16
A100	40	GCP	a2-highgpu-1g	11.0.3	8.0.2	450.51.06	1.7.0a0+8deb4fe	-	12	85
TPU v3	16	GCP	n1-highmem-8	-	-	-	1.7.0a0+626e410	1.6+8af57fb	8	52

our benchmarks. All four workloads aim at maximizing the validation accuracy on their corresponding datasets. Each workload tunes eight independent hyper-parameters. We discuss the detailed setup of these benchmarks in Appendix H.

Experimental Setup Our experiments are performed on two types of ML accelerators (NVIDIA GPUs and Google TPUs) including the most recent three generations of GPUs and the latest available generation of TPUs: (i) Volta-based V100 (NVIDIA, 2020k), (ii) Turing-based RTX6000 (NVIDIA, 2020i), and (iii) very recent Ampere-based A100 (NVIDIA, 2020a),⁴ (iv) TPU v3 (Google, 2020a). We provide the detailed specifications in Table 4.

Baselines We use *hyper-parameter tuning* (including learning rate, learning rate schedule, and optimizer settings) as the use case for our repetitive single-accelerator training jobs under experimentation. We compare HFTA with the following four SOTA baselines. (1) *Serial*: each training job is executed on a single accelerator. This scheme is employed by most hyper-parameter tuning frameworks (Weights&Biases, 2020; Li, 2020). (2) *Concurrent*: multiple training jobs are executed as independent processes on the same GPU. In this case, the kernels from different processes are *time-multiplexed*, but can *not* execute concurrently on the same GPU (without the help of MPS or other hardware features). This scheme is used when MPS is not preferable due to reasons related to infrastructure and/or security (e.g., custom-built infrastructure or CUPTI tools that are not compatible with MPS). (3) *MPS*: similar to *concurrent*, except the independent processes are executed via MPS. (4) *MIG*: similar to *concurrent*, except the independent processes are executed via MIG. This scheme is currently only available on the A100 GPUs. We use *concurrent*, *MPS*, and *MIG* only on GPUs since TPUs do not support running concurrent processes as of now. We do not evaluate the major related prior work, HiveMind (Narayanan et al., 2018a), since it is both close-sourced and implemented on a different ML framework (TensorFlow). We provide the detailed qualitative comparison against HiveMind in Section 6.

Metrics We use the *per-device training throughput* as our key performance metric to compare HFTA against our baselines since HFTA has no impact on the model convergence. We calculate this throughput by measuring the end-to-end training latency of (i) 10 epochs for both classification and segmentation tasks on PointNet; and (2) 5 epochs, 1000 iterations per epoch on DCGAN (enough for these workloads

to enter the execution steady state). We skip the first epoch on GPUs and the first two epochs on TPUs to warm up the hardware properly before making any measurements. We repeat each experiment three times and report the average, minimum, and maximum per experiment.

To measure the effect of each technique on the hardware utilization, we use the `sm_active` and `sm_occupancy` performance counters that represent the SM temporal and spatial utilization, respectively. We also use the `tensor_active` performance counter to measure the TC temporal utilization (NVIDIA, 2020d). Details on these performance counters can be found in Appendix F.

5 EVALUATION

Our evaluation results on the major benchmarks (i.e., PointNet classification task, PointNet segmentation task, and DCGAN) are thoroughly analyzed here, including end-to-end training performance on GPUs (Section 5.1) and TPUs (Section 5.2). We also analyze key GPU hardware performance counters to explain why HFTA achieves significantly better training performance (Section 5.3). We discuss the results on our secondary benchmarks (i.e., ResNet-18, MobileNetV3-Large, Transformer, and BERT-Medium) in Appendix I. Finally, we showcase HFTA’s potential to significantly improve the hardware utilization for existing hyper-parameter tuning algorithms (Section 5.4).

5.1 End-to-end Training Performance on GPUs

V100 Results To compare the HFTA’s end-to-end training performance with other alternatives (i.e., *serial*, *concurrent*, *MPS*), Figure 4a, 4b and 4c plot the per-GPU normalized training throughput on the V100 GPUs (Volta architecture (NVIDIA, 2017)) with the PointNet classification task, PointNet segmentation task, and DCGAN respectively. We normalize the throughput for each experiment by the respective FP32 *serial* baseline. We show both FP32 and AMP (Huang et al., 2020) training results for each experiment. Each curve grows as we increase the number of models that either co-run together (for the *concurrent* and *MPS* baselines) or run in the fused form with HFTA. Each curve “stops” when it reaches the maximum number of models before the GPU runs out of memory. Based on these figures, we make several major observations:

First, *HFTA achieves significantly higher peak throughput than all baselines*; specifically, $4.29\times$ to $5.02\times$ over *serial*, $2.01\times$ to $4.87\times$ over *concurrent* and $2.03\times$ to $4.50\times$ over *MPS*. The significant throughput improvement is due to a much higher achieved utilization in both compute cores

⁴Using GCP A2 Alpha version instances.

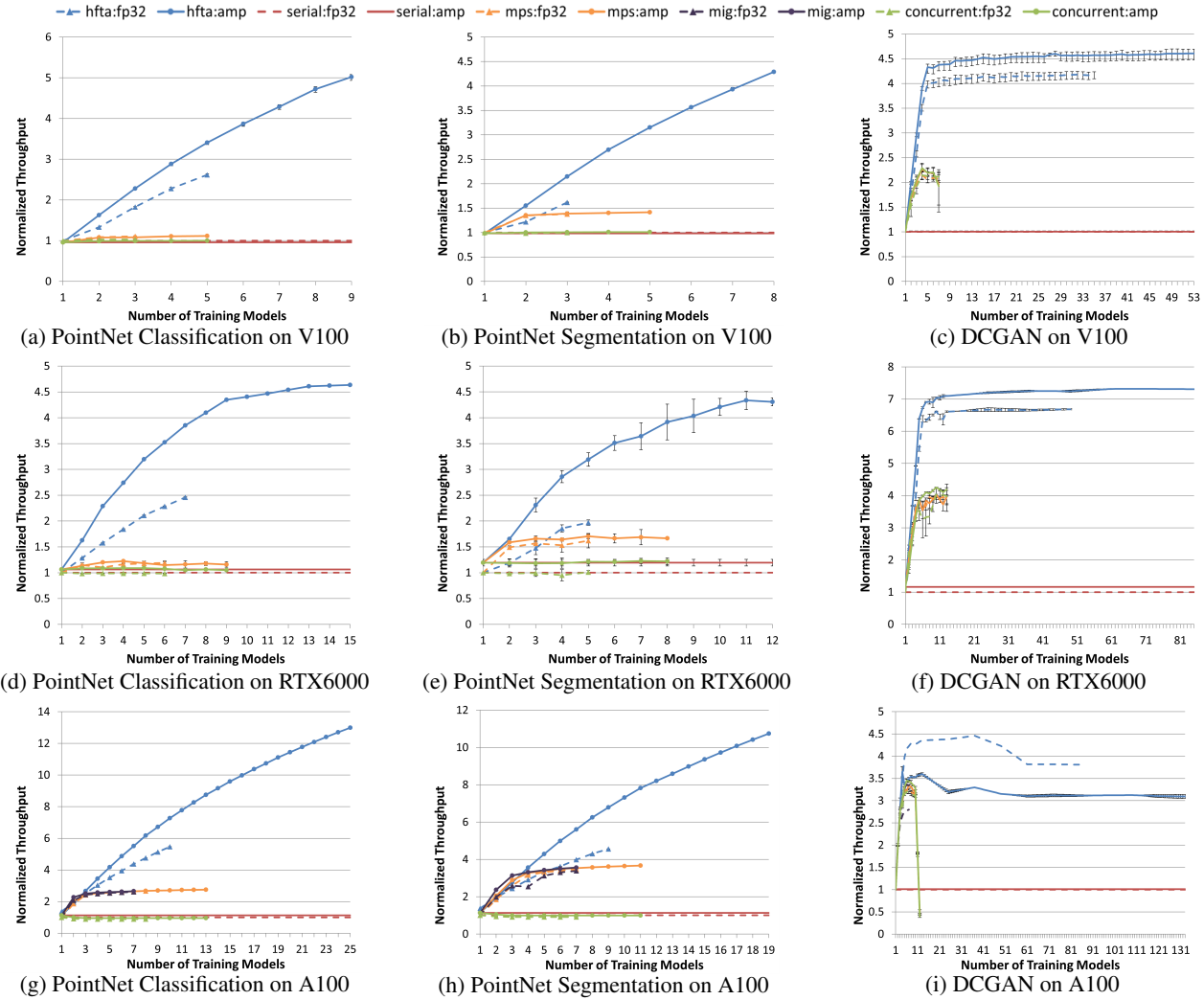


Figure 4. The normalized training throughput as we increase the number of models sharing the same GPU.

(details in Section 5.3) and GPU memory (discussed in the next observation).

Second, *HFTA enables more models to share the same GPU than MPS and concurrent*; specifically, up to $1.80\times$ on the PointNet classification task, up to $1.60\times$ on the segmentation task and up to $7.57\times$ on DCGAN. This is because HFTA does not duplicate the GPU memory overhead as we explain in Section 5.3.

Third, *as we increase the number of models sharing the same GPU, the throughput of HFTA scales up and, in some cases, plateaus eventually*. This is because using HFTA, the SM and TC utilization increases with the number of co-executing models (as we explain in Section 5.3). In contrast, *MPS and concurrent* either (i) plateau at a smaller number of models with a lower throughput, as we observe in Figure 4a and 4b, or (ii) even experience performance degradation as we observe in Figure 4c due to host resource (e.g., CPUs, disk I/O bandwidth, and/or memory) contention among many training processes.

Fourth, *even with the same number of models sharing the same GPU, HFTA often achieves higher throughput than all baselines*. The maximum speedups range from $1.62\times$ to $3.41\times$ over *concurrent* and $1.17\times$ to $3.05\times$ over *MPS*.

Fifth, *HFTA can better exploit computing power from advanced hardware features such as TCs used during AMP training compared to the baselines*. Specifically, the maximum speedup of AMP training over FP32 is $2.65\times$ with HFTA, but only $1.00\times$ for *serial*, $1.07\times$ for *concurrent*, and $1.06\times$ for *MPS*.

Therefore, we conclude that HFTA can significantly outperform major hardware-based sharing alternatives in improving hardware utilization and, as a result, improve the throughput of emerging ML models during repetitive single-accelerator training.

RTX6000 and A100 Results To check whether HFTA’s significant performance gains are general across different GPU architectures (e.g., Turing (NVIDIA, 2018) and Am-

pere (NVIDIA, 2020b)), we conduct the same set of experiments on the RTX6000 (Figure 4d, 4e and 4f respectively) and the A100 (Figure 4g, 4h and 4i respectively) while adding the extra *MIG* baseline for the A100. The general trends in these figures are similar to those we observe for V100. To simplify the comparison, for each workload on each GPU, Table 5 presents the peak throughput speedups of HFTA over the baselines, while Appendix G presents (i) the maximum throughput speedups of HFTA over the baselines given a fixed number of models, and (ii) the maximum AMP training throughput speedups over FP32 for both HFTA and the baselines. In addition, we make the following new observations:

First, both RTX6000 and A100 have higher GPU memory (HBM) capacities than V100 (24 GB and 40 GB vs. 16 GB); therefore, *both HFTA and the baselines can co-run more models on the same RTX6000/A100 compared with V100*. For example, AMP training of the PointNet classification task via HFTA can run up to 15/25 models on RTX6000/A100 vs. 9 on V100.

Second, since A100 has more compute capability and a larger GPU memory capacity than V100, the comparison of Figure 4g vs. 4a and 4h vs. 4b reveals that *HFTA not only fits more models on the same hardware, but also achieves a higher peak throughput speedup over the baselines on A100 than on V100* (e.g., for PointNet segmentation task, the peak throughput speedup over serial is as high as $9.48\times$ on A100 vs. $4.29\times$ on V100).

Third, we observe one anomaly in DCGAN training on A100 (Figure 4i) where HFTA’s FP32 throughput is higher than that of AMP. After profiling the AMP run of this experiment via the PyProf (Agrawal & Kolodziej, 2020) tool, we pinpoint a few suspicious cuDNN-related FP32 kernels (which are supposed to be replaced by the equivalent TC kernels) in the backward pass. Since the Ampere architecture and the corresponding versions of cuDNN/PyTorch are very recently released, and we do not observe similar problems on older cuDNN/PyTorch versions for V100 and RTX6000, we believe that this issue is temporary due to the insufficient optimization in some of the new cuDNN kernels for A100. We hope it will be addressed in future cuDNN releases/fixes and we will be able to update the results accordingly.

Fourth, we notice that *on A100, the MIG partitioning (only up to 7 GIs) can be too coarse-grained*. As we observe in Figure 4g, 4h and 4i, both *MPS* and *concurrent* could often share the A100 with more than seven models.

Therefore, we conclude that HFTA’s performance generally scales well with the compute and memory capabilities of modern GPUs. We observe higher performance benefits in the newer GPU architectures that would otherwise suffer more significantly from the hardware under-utilization

Table 5. The peak training throughput speedups of HFTA over the baselines. For each experiment, the higher throughput between FP32 and AMP is used in the calculation. The detailed breakdown between FP32 and AMP is included in Appendix G.

Benchmark		PointNet Classification	PointNet Segmentation	DCGAN
V100	<i>serial</i>	5.02	4.29	4.59
	<i>concurrent</i>	4.87	4.24	2.01
	<i>MPS</i>	4.50	3.03	2.03
RTX6000	<i>serial</i>	4.36	3.63	6.29
	<i>concurrent</i>	4.26	3.54	1.72
	<i>MPS</i>	3.79	2.54	1.82
A100	<i>serial</i>	11.50	9.48	4.41
	<i>concurrent</i>	12.98	10.26	1.29
	<i>MPS</i>	4.72	2.93	1.33
	<i>MIG</i>	4.88	3.02	1.33

when training without HFTA (as we qualitatively discuss in Section 2.1 and empirically show in Appendix G).

5.2 End-to-end Training Performance on TPUs

As we aim to build a general solution that works for different ML accelerators, we also evaluate HFTA on an entirely different type of accelerator: Google TPU v3. Figure 5 plots the per-core training throughput for *serial* vs. HFTA on the PointNet classification and DCGAN experiments on TPU v3, normalized by the throughput of the respective *serial* baseline. Similar to previous results on GPUs, each HFTA curve shows how the normalized throughput increases with the number of models sharing the same TPU (until the fused models can not fit into the TPU HBM memory). We make three major observations from these figures.

First, *HFTA achieves $4.93\times$ / $15.13\times$ higher peak throughput than serial on the PointNet classification / DCGAN*.

Second, we observe that *for DCGAN, HFTA can sometimes achieve “super-linear” speedups*. Our current investigation concludes that the most likely cause of such a behaviour is the tensor padding added in the *serial* baseline by the XLA (Google, 2020b) compiler (Google, 2020d), making this baseline weaker than it should be otherwise.

Additionally, we also investigate the HFTA’s potential on the PointNet segmentation task. Unfortunately, HFTA currently achieves a less impressive $1.20\times$ speedup over the *serial* baseline, which we attribute to the PointNet segmentation variant having many non-GEMM-based operators that intrinsically do *not* map well to systolic arrays by the XLA compiler. Deeper analysis, however, is limited due to the xprof (Google, 2020f) tool, just recently released, do not directly support PyTorch/XLA. We will perform deeper analysis of this problem and research potential solutions as soon as a proper version of the profiler is released.

5.3 In-depth Performance Analysis

Using PointNet classification task as a case study, we perform deeper analysis by profiling GPU hardware performance counters to explain why HFTA can share the same GPU with more training workloads and achieves higher training throughput than the baselines.

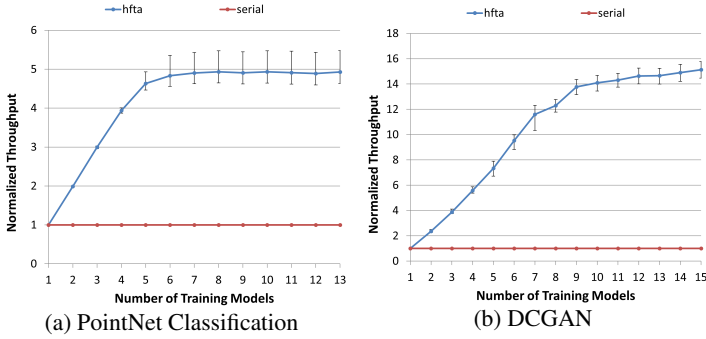


Figure 5. The normalized training throughput as we increase the number of models sharing (via HFTA) the same TPU v3 core.

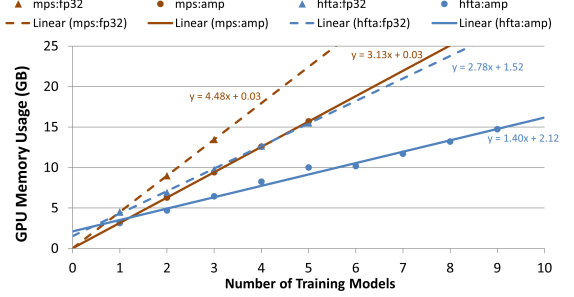


Figure 6. GPU Memory Footprints of MPS and HFTA for PointNet classification task as we increase the number of models sharing the same V100.

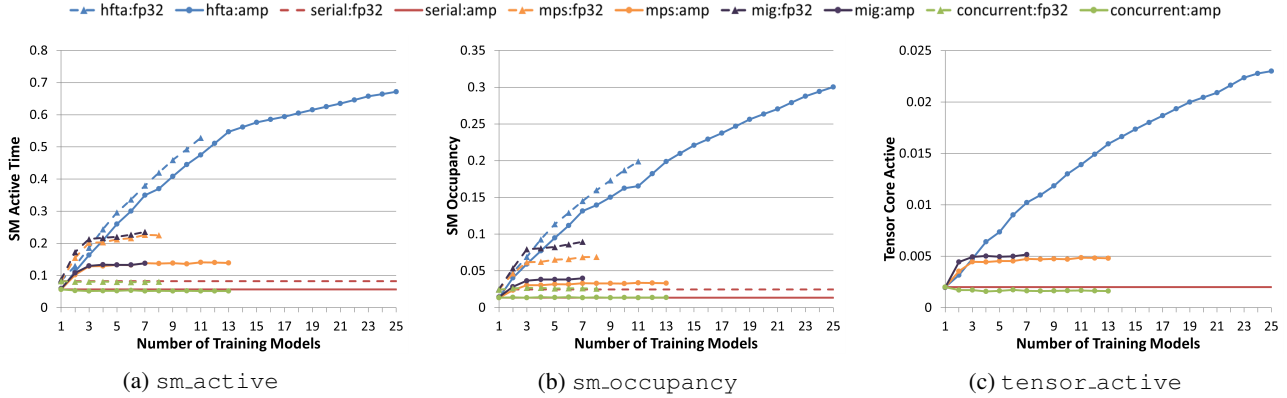


Figure 7. The hardware performance counters for PointNet classification task as we increase the number of models sharing the same A100.

Figure 6 plots the GPU memory footprint of MPS and HFTA as we increase the number of models sharing the same V100 GPU⁵ and the linear regression lines fitted on those measurements. Training models in independent processes duplicates the associated GPU memory overheads (reserved by the DL framework stack (Gross et al., 2019)), which is a challenge that HFTA addresses. Thus, we can observe that: (1) MPS’s linear regression lines pass through the (0, 0) coordinate and have higher slopes than HFTA’s; and (2) the intercepts of HFTA’s linear regression lines essentially represent the exact amounts of memory overhead which are 1.52GB for FP32 training and 2.12GB for AMP.

Figure 7 plots the `sm_active`, `sm_occupancy`, and `tensor_active` of HFTA and the baselines as we increase the number of models sharing the same A100 GPU.⁶ We can observe: (1) HFTA’s SM and TC utilization keeps scaling up as we fuse more models horizontally. (2) MIG’s and MPS’s SM and TC utilization plateaus at a smaller number of models and lower utilization, which supports our qualitative reasoning in Section 2.2 that both leave significant potential of training performance unharnessed; (3) `concurrent`’s SM and TC utilization stays the same as `serial` because the kernels from parallel processes can not execute concurrently without MPS or MIG.

⁵The trends on RTX6000 and A100 are consistent with V100.

⁶V100 results are similar and shown in Appendix G.

5.4 Overall Cost Saving for Tuning Algorithms

To demonstrate that HFTA can be efficient in improving the hardware utilization for existing hyper-parameter tuning algorithms, Figure 8 lists the total GPU hour cost of tuning eight hyper-parameters via HFHT for the PointNet and MobileNet classification tasks on the V100 GPU using two tuning algorithms (random search (Bergstra & Bengio, 2012) and Hyperband (Li et al., 2018)) and four job schedulers (`serial`, `concurrent`, `MPS`, and `HFTA`). We make two major observations from this figure.

First, *HFTA can reduce the total GPU hour cost by up to 5.10× and lead to significantly better hardware utilization than all other baselines.*

Second, as we theoretically discuss in Appendix E, *random search benefits more from HFTA than Hyperband.* This is because, during certain iterations, Hyperband proposes to run *many* epochs on just a *few* sets of hyper-parameters. Thus, within such iterations, Hyperband generates not enough parallel jobs to either share the GPU with MPS or to be fused by HFTA. Therefore, such iterations become the bottleneck of the total cost when tuning is conducted with a job scheduler based on hardware sharing.

6 RELATED WORKS

Major prior works on DL job fusion (Liu et al., 2020; Narayanan et al., 2018b;a) suffer from three key weaknesses:

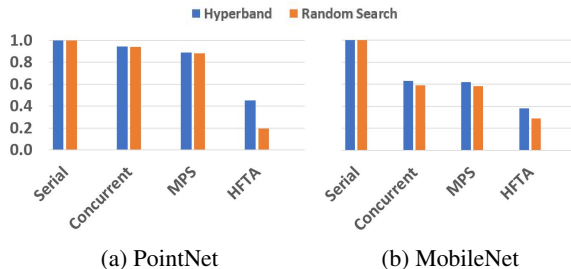


Figure 8. Total GPU hours of four hyper-parameter tuning workloads on V100. For each algorithm and scheduler, we show the lower total GPU hours between the FP32 and AMP training.

(i) avoiding directly addressing hardware under-utilization, (ii) strongly depending on the CUDA stream primitive (Harris, 2015), a generic GPU-sharing method but inefficient for repetitive training jobs, and (iii) employing very restricted fusion schemes that are ineffective in practice. We discuss these prior works in detail below.

pack (Liu et al., 2020) merges TensorFlow (Abadi et al., 2016) graphs from multiple training jobs into a single graph to amortize *only* the IO and data preprocessing cost, but does not address the hardware under-utilization from the model forward and backward passes.

Furthermore, ModelBatch (Narayanan et al., 2018b) attempts to parallelize the kernel launches from multiple training jobs via CUDA streams (the CUDA programming interface of Hyper-Q (Bradley, 2007)), which suffers from similar pitfalls of runtime overhead duplication as MPS.

Although *intra*-model vertical and horizontal fusion of DL operators have been studied extensively by many prior works (Appleyard et al., 2016; Gray et al., 2017; Vasilache et al., 2018; Rotem et al., 2018; Chen et al., 2018; Jia et al., 2019), *inter*-model horizontal fusion has only been explored in extremely limited depth: HiveMind (Narayanan et al., 2018a) proposes fusion schemes for 1) non-stateful operators with the same shapes, 2) stateful operators that share the same weights, and 3) stateful operators that share the same shapes and inputs. Unfortunately, condition 2) is rarely applicable to training workloads since each individual model has its own weights, while condition 3) usually only applies to the first operator in a DL model since the following operators will have different inputs, leaving most of the fusion opportunities completely untapped. Besides, HiveMind does not demonstrate any performance improvement over MPS as it also relies on CUDA streams to extract utilization when its fusion scheme becomes ineffective. Therefore, HiveMind approach is hard to generalize to accelerators with no hardware-specific sharing features (e.g., TPUs).

In contrast, HFTA can fuse any operators of the same types and shapes across training jobs, which generally leads to full inter-model fusions. Moreover, HFTA demonstrates significant performance improvement against the existing

widely-adopted generic hardware-based sharing approaches (e.g., MPS and MIG) since operator fusion does not possess the same shortcomings of those approaches, as we show in Section 2.2. Finally, HFTA requires no hardware or DL framework stack modifications and applies to any existing hardware backends, including GPUs, TPUs, and any other accelerators that the major DL frameworks support.

In parallel with our work: Rammer (Ma et al., 2020) proposes a data flow graph compiler that enables hardware sharing via operator and accelerator abstractions which requires special operator implementations (e.g., using the Persistent Thread programming model (Gupta et al., 2012) for CUDA), and focuses mostly on intra-model horizontal fusion and inference workloads. Retiarri (Zhang et al., 2020) hints that observations similar to ours are possible, but does not focus on exploring this idea in depth.

7 CONCLUSION

In this work, we learn from the GPU cluster usage analysis that repetitive single-accelerator training jobs (e.g., for hyper-parameters tuning) often dominate cluster-wide hardware resource usage and can severely under-utilize the hardware. To address this challenge, we observe that these jobs possess unique characteristics which enables the inter-model horizontal fusion. Therefore, we propose the HFTA (DL framework extension) library that horizontally fuses the models deeply down to operators with a minimal extra effort from DL researchers and practitioners, significantly improving the hardware utilization of these workloads by simultaneously training many models on the same accelerator. On six highly impactful DL models, HFTA achieves up to $15.13\times$ higher training throughput than running each job on a separate accelerator, a common practice employed by hyper-parameter tuning frameworks. We continue to expand the coverage of HFTA with more operators, optimizers, and learning rate schedulers, and to investigate how existing DL frameworks, hyper-parameter tuning and model architecture search algorithms can be adjusted to extract more performance from hardware sharing via HFTA. We hope our work inspires future research on assisting ML researchers and developers with limited optimization experience to better utilize the hardware for their novel DL models.

ACKNOWLEDGEMENTS

We want to especially thank Suvinay Subramanian for TPU-related issues and discussions. We want to thank Xiaodan (Serina) Tan, Suvinay Subramanian, James Gleeson, Anand Jayarajan, and Garth Gibson for their constructive feedback during the development of this work. We want to thank Google for TPU credits and early accesses to the GCP A2 Alpha version instances. This project was supported in part by the Canada Foundation for Innovation JELF grant, NSERC Discovery grant, AWS Machine Learning Research Award, and Facebook Faculty Research Award.

REFERENCES

- Abadi, M., Barham, P., Chen, J., Chen, Z., Davis, A., Dean, J., Devin, M., Ghemawat, S., Irving, G., Isard, M., Kudlur, M., Levenberg, J., Monga, R., Moore, S., Murray, D. G., Steiner, B., Tucker, P., Vasudevan, V., Warden, P., Wicke, M., Yu, Y., and Zheng, X. Tensorflow: A system for large-scale machine learning. In *12th USENIX Symposium on Operating Systems Design and Implementation (OSDI)*, pp. 265–283, 2016.
- Agrawal, A. and Kolodziej, M. Pyprof: Automating end-to-end pytorch profiling. <https://developer.download.nvidia.com/video/gputechconf/gtc/2020/presentations/s21143-automating-end-to-end-pytorch-profiling.pdf>, 2020. Accessed: 2020-09-17.
- Akkus, Z., Galimzianova, A., Hoogi, A., Rubin, D., and Erickson, B. Deep learning for brain mri segmentation: State of the art and future directions. *Journal of digital imaging*, 30, 06 2017.
- Amodei, D., Hernandez, D., Sastry, G., Clark, J., Brockman, G., and Sutskever, I. Ai and compute. <https://openai.com/blog/ai-and-compute/>, 2018. Accessed: 2020-09-13.
- Appleyard, J., Kociský, T., and Blunsom, P. Optimizing performance of recurrent neural networks on gpus. *CoRR*, abs/1604.01946, 2016.
- Bergstra, J. and Bengio, Y. Random search for hyperparameter optimization. *J. Mach. Learn. Res.*, 13: 281–305, February 2012.
- Bergstra, J., Bardenet, R., Bengio, Y., and Kégl, B. Algorithms for hyper-parameter optimization. In *Advances in Neural Information Processing Systems 24 (NIPS)*, pp. 2546–2554, 2011.
- Bradley, T. Hyper-q example. Technical report, 2007. Accessed: 2020-09-17.
- Brock, A., Donahue, J., and Simonyan, K. Large scale GAN training for high fidelity natural image synthesis. In *7th International Conference on Learning Representations, (ICLR)*, 2019.
- Charrez, D. Neurips 2019 stats. <https://medium.com/@dcharrezt/neurips-2019-stats-c91346d31c8f>, 2019. Accessed: 2020-09-17.
- Chen, T., Li, M., Li, Y., Lin, M., Wang, N., Wang, M., Xiao, T., Xu, B., Zhang, C., and Zhang, Z. Mxnet: A flexible and efficient machine learning library for heterogeneous distributed systems. *CoRR*, abs/1512.01274, 2015.
- Chen, T., Xu, B., Zhang, C., and Guestrin, C. Training deep nets with sublinear memory cost. *CoRR*, abs/1604.06174, 2016.
- Chen, T., Moreau, T., Jiang, Z., Zheng, L., Yan, E., Shen, H., Cowan, M., Wang, L., Hu, Y., Ceze, L., Guestrin, C., and Krishnamurthy, A. TVM: An automated end-to-end optimizing compiler for deep learning. In *13th USENIX Symposium on Operating Systems Design and Implementation (OSDI)*, pp. 578–594, October 2018.
- Coleman, C. A., Narayanan, D., Kang, D., Zhao, T., Zhang, J., Nardi, L., Bailis, P., Olukotun, K., Ré, C., and Zaharia, M. Dawnbench : An end-to-end deep learning benchmark and competition. 2017.
- Devlin, J., Chang, M., Lee, K., and Toutanova, K. BERT: pre-training of deep bidirectional transformers for language understanding. In Burstein, J., Doran, C., and Solorio, T. (eds.), *Proceedings of the 2019 Conference of the North American Chapter of the Association for Computational Linguistics: Human Language Technologies, NAACL-HLT 2019, Minneapolis, MN, USA, June 2-7, 2019, Volume 1 (Long and Short Papers)*, pp. 4171–4186. Association for Computational Linguistics, 2019. doi: 10.18653/v1/n19-1423.
- Elangovan, A. Optimizing i/o for gpu performance tuning of deep learning training in amazon sagemaker. <https://aws.amazon.com/blogs/machine-learning/optimizing-i-o-for-gpu-performance-tuning-of-deep-learning-training-in-amazon-sagemaker/>, 2020. Accessed: 2020-10-09.
- Elsken, T., Metzen, J. H., and Hutter, F. Neural architecture search: A survey. *J. Mach. Learn. Res.*, 20:55:1–55:21, 2019.
- fastai. Working with gpu. <https://docs.fast.ai/dev/gpu>, 2020. Accessed: 2020-10-09.
- Google. Cloud tpu. <https://cloud.google.com/tpu>, 2020a. Accessed: 2020-09-17.
- Google. Pytorch/xla. <https://github.com/pytorch/xla>, 2020b. Accessed: 2020-09-17.
- Google. System architecture. <https://cloud.google.com/tpu/docs/system-architecture>, 2020c. Accessed: 2020-09-17.
- Google. Troubleshooting. <https://cloud.google.com/tpu/docs/troubleshooting>, 2020d. Accessed: 2020-09-17.
- Google. Xla: Optimizing compiler for machine learning. <https://www.tensorflow.org/xla>, 2020e. Accessed: 2020-09-17.

- Google. Using cloud tpu tools. <https://cloud.google.com/tpu/docs/cloud-tpu-tools>, 2020f. Accessed: 2020-09-17.
- Gray, A., Gottbrath, C., Olson, R., and Prasanna, S. Deploying deep neural networks with nvidia tensorrt. <https://developer.nvidia.com/blog/deploying-deep-learning-nvidia-tensorrt/>, 2017. Accessed: 2020-09-17.
- Gross, S., Chintala, S., and Jones, A. Couple hundred mb are taken just by initializing cuda #20532. <https://github.com/pytorch/pytorch/issues/20532>, 2019. Accessed: 2020-09-17.
- Gupta, K., Stuart, J. A., and Owens, J. D. A study of persistent threads style gpu programming for gpgpu workloads. In *2012 Innovative Parallel Computing (InPar)*, pp. 1–14, 2012. doi: 10.1109/InPar.2012.6339596.
- Harris, M. Gpu pro tip: Cuda 7 streams simplify concurrency. <https://developer.nvidia.com/blog/gpu-pro-tip-cuda-7-streams-simplify-concurrency/>, 2015. Accessed: 2020-09-13.
- He, H. The state of machine learning frameworks in 2019. *The Gradient*, 2019.
- He, K., Zhang, X., Ren, S., and Sun, J. Deep residual learning for image recognition. In *2016 IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, pp. 770–778, 2016.
- Howard, A., Zhu, M., Chen, B., Kalenichenko, D., Wang, W., Weyand, T., Andreetto, M., and Adam, H. Mobilenets: Efficient convolutional neural networks for mobile vision applications. *CoRR*, abs/1704.04861, 2017.
- Howard, A., Sandler, M., Chen, B., Wang, W., Chen, L., Tan, M., Chu, G., Vasudevan, V., Zhu, Y., Pang, R., Adam, H., and Le, Q. Searching for mobilenetv3. In *2019 IEEE/CVF International Conference on Computer Vision (ICCV)*, pp. 1314–1324, 2019. doi: 10.1109/ICCV.2019.00140.
- Huang, M., Tekur, C., and Carilli, M. Introducing native pytorch automatic mixed precision for faster training on nvidia gpus. <https://pytorch.org/blog/accelerating-training-on-nvidia-gpus-with-pytorch-automatic-mixed-precision/>, 2020. Accessed: 2020-09-17.
- Jamieson, K. and Talwalkar, A. Non-stochastic best arm identification and hyperparameter optimization. In Gretton, A. and Robert, C. C. (eds.), *Proceedings of the 19th International Conference on Artificial Intelligence and Statistics*, volume 51 of *Proceedings of Machine Learning Research*, pp. 240–248, Cadiz, Spain, 09–11 May 2016. PMLR.
- Jayarajan, A., Wei, J., Gibson, G., Fedorova, A., and Pekhimenko, G. Priority-based parameter propagation for distributed DNN training. In Talwalkar, A., Smith, V., and Zaharia, M. (eds.), *Proceedings of Machine Learning and Systems 2019 (MLSys)*, 2019.
- Jia, Z., Thomas, J. J., Warszawski, T., Gao, M., Zaharia, M., and Aiken, A. Optimizing DNN computation with relaxed graph substitutions. In *Proceedings of Machine Learning and Systems 2019 (MLSys)*, 2019.
- Jouppi, N. P., Young, C., Patil, N., Patterson, D., Agrawal, G., Bajwa, R., Bates, S., Bhatia, S., Boden, N., Borchers, A., Boyle, R., Cantin, P., Chao, C., Clark, C., Coriell, J., Daley, M., Dau, M., Dean, J., Gelb, B., Ghaemmaghami, T. V., Gottipati, R., Gulland, W., Hagmann, R., Ho, C. R., Hogberg, D., Hu, J., Hundt, R., Hurt, D., Ibarz, J., Jaffey, A., Jaworski, A., Kaplan, A., Khaitan, H., Killebrew, D., Koch, A., Kumar, N., Lacy, S., Laudon, J., Law, J., Le, D., Leary, C., Liu, Z., Lucke, K., Lundin, A., MacKean, G., Maggiore, A., Mahony, M., Miller, K., Nagarajan, R., Narayanaswami, R., Ni, R., Nix, K., Norrie, T., Omernick, M., Penukonda, N., Phelps, A., Ross, J., Ross, M., Salek, A., Samadiani, E., Severn, C., Sizikov, G., Snelham, M., Souter, J., Steinberg, D., Swing, A., Tan, M., Thorson, G., Tian, B., Toma, H., Tuttle, E., Vasudevan, V., Walter, R., Wang, W., Wilcox, E., and Yoon, D. H. In-datacenter performance analysis of a tensor processing unit. In *2017 ACM/IEEE 44th Annual International Symposium on Computer Architecture (ISCA)*, pp. 1–12, 2017.
- Keskar, N. S., Mudigere, D., Nocedal, J., Smelyanskiy, M., and Tang, P. T. P. On large-batch training for deep learning: Generalization gap and sharp minima. In *5th International Conference on Learning Representations, (ICLR)*, 2017.
- Kim, J. Bert-pytorch. <https://github.com/coderimo/BERT-pytorch>, 2018. Accessed: 2020-11-18.
- Kingma, D. P. and Ba, J. Adam: A method for stochastic optimization. In *3rd International Conference on Learning Representations, (ICLR)*, 2015.
- Krizhevsky, A. Learning multiple layers of features from tiny images. Technical report, 2009. URL <https://www.cs.toronto.edu/~kriz/learning-features-2009-TR.pdf>.
- Krizhevsky, A., Sutskever, I., and Hinton, G. E. Imagenet classification with deep convolutional neural networks. In *Advances in Neural Information Processing Systems 24 (NIPS)*, pp. 1097–1105. 2012.
- Kukanur, M. Nvidia data center gpu manager simplifies cluster administration. <https://developer.nvidia.com/blog/nvidia-data-center-gpu>

- manager-cluster-administration/, 2016. Accessed: 2020-09-17.
- Kumar, N. Google breaks ai performance records in mlperf with world’s fastest training supercomputer. <https://cloud.google.com/blog/products/ai-machine-learning/google-breaks-ai-performance-records-in-mlperf-with-world-s-fastest-training-supercomputer>, 2020. Accessed: 2020-09-17.
- Levenshtein, V. I. Binary codes capable of correcting deletions, insertions and reversals. *Soviet physics. Doklady*, 10:707–710, 1966.
- Li, L. Why does no one use advanced hyperparameter tuning? <https://determined.ai/blog/why-does-no-one-use-advanced-hp-tuning/>, 2020. Accessed: 2020-10-09.
- Li, L., Jamieson, K., DeSalvo, G., Rostamizadeh, A., and Talwalkar, A. Hyperband: A novel bandit-based approach to hyperparameter optimization. *Journal of Machine Learning Research*, 18(185):1–52, 2018. URL <http://jmlr.org/papers/v18/16-558.html>.
- Li, S., Zhao, Y., Varma, R., Salpekar, O., Noordhuis, P., Li, T., Paszke, A., Smith, J., Vaughan, B., Damania, P., and Chintala, S. Pytorch distributed: Experiences on accelerating data parallel training. *Proc. VLDB Endow.*, 13:3005–3018, 2020.
- Liaw, R., Liang, E., Nishihara, R., Moritz, P., Gonzalez, J. E., and Stoica, I. Tune: A research platform for distributed model selection and training. *arXiv preprint arXiv:1807.05118*, 2018.
- Lin, Y., Han, S., Mao, H., Wang, Y., and Dally, B. Deep gradient compression: Reducing the communication bandwidth for distributed training. In *6th International Conference on Learning Representations, (ICLR)*, 2018.
- Lin, Y., Dhar, S., Li, W., Ren, H., Khailany, B., and Pan, D. Z. Dreampiace: Deep learning toolkit-enabled gpu acceleration for modern vlsi placement. In *56th ACM/IEEE Design Automation Conference (DAC)*, pp. 1–6, June 2019.
- Liu, R., Krishnan, S., Elmore, A. J., and Franklin, M. Understanding and optimizing packed neural network training for hyper-parameter tuning. *CoRR*, abs/2002.02885, 2020.
- Lustig, D. and Martonosi, M. Reducing gpu offload latency via fine-grained cpu-gpu synchronization. In *Proceedings of the IEEE 19th International Symposium on High Performance Computer Architecture (HPCA)*, pp. 354–365, 2013.
- Ma, L., Xie, Z., Yang, Z., Xue, J., Miao, Y., Cui, W., Hu, W., Yang, F., Zhang, L., and Zhou, L. Rammer: Enabling holistic deep learning compiler optimizations with rtasks. In *14th USENIX Symposium on Operating Systems Design and Implementation (OSDI 20)*, pp. 881–897. USENIX Association, November 2020.
- Markidis, S., Chien, S. W. D., Laure, E., Peng, I. B., and Vetter, J. S. Nvidia tensor core programmability, performance precision. In *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pp. 522–531, 2018.
- Mattson, P., Cheng, C., Damos, G., Coleman, C., Micikevicius, P., Patterson, D., Tang, H., Wei, G.-Y., Bailis, P., Bittorf, V., Brooks, D., Chen, D., Dutta, D., Gupta, U., Hazelwood, K., Hock, A., Huang, X., Kang, D., Kanter, D., Kumar, N., Liao, J., Narayanan, D., Oguntebi, T., Pekhimenko, G., Pentecost, L., Janapa Reddi, V., Robie, T., St John, T., Wu, C.-J., Xu, L., Young, C., and Zaharia, M. Mlperf training benchmark. In *Proceedings of Machine Learning and Systems 2020 (MLSys)*, volume 2, pp. 336–349. 2020.
- Merity, S., Xiong, C., Bradbury, J., and Socher, R. Pointer sentinel mixture models. In *5th International Conference on Learning Representations, ICLR 2017, Toulon, France, April 24-26, 2017, Conference Track Proceedings*, 2017.
- Narayanan, D., Santhanam, K., Phanishayee, A., and Zaharia, M. Accelerating deep learning workloads through efficient multi-model execution. In *NeurIPS Workshop on Systems for Machine Learning*, December 2018a.
- Narayanan, D., Santhanam, K., and Zaharia, M. Accelerating model search with model batching (extended abstract). In *SysML Conference 2018*, 2018b.
- Naumov, M., Mudigere, D., Shi, H. M., Huang, J., Sundaraman, N., Park, J., Wang, X., Gupta, U., Wu, C., Azzolini, A. G., Dzhulgakov, D., Malleevich, A., Cherniavskii, I., Lu, Y., Krishnamoorthi, R., Yu, A., Kondratenko, V., Pereira, S., Chen, X., Chen, W., Rao, V., Jia, B., Xiong, L., and Smelyanskiy, M. Deep learning recommendation model for personalization and recommendation systems. *CoRR*, abs/1906.00091, 2019.
- NVIDIA. nvidia-smi documentation. <http://developer.download.nvidia.com/compute/DCGM/docs/nvidia-smi-367.38.pdf>, 2016. Accessed: 2020-10-09.
- NVIDIA. Nvidia tesla v100 gpu architecture. Technical Report WP-08608-001_v1.1, 2017. Accessed: 2020-09-17.

- NVIDIA. Nvidia turing architecture whitepaper. Technical Report WP-09183-001_v01, 2018. Accessed: 2020-09-17.
- NVIDIA. Nvidia a100 tensor core gpu. <https://www.nvidia.com/en-us/data-center/a100/>, 2020a. Accessed: 2020-09-17.
- NVIDIA. Nvidia a100 tensor core gpu architecture. Technical report, 2020b. Accessed: 2020-09-17.
- NVIDIA. cudnn developer guide. <https://docs.nvidia.com/deeplearning/cudnn/developer-guide/index.html#grouped-convolutions>, 2020c. Accessed: 2020-09-17.
- NVIDIA. Dcgm library api reference manual. https://docs.nvidia.com/datacenter/dcgm/latest/dcgm-api/group__dcgmFieldIdentifiers.html#group__dcgmFieldIdentifiers, 2020d. Accessed: 2020-09-17.
- NVIDIA. Nvidia dlss 2.0: A big leap in ai rendering. www.nvidia.com/en-us/geforce/news/nvidia-dlss-2-0-a-big-leap-in-ai-rendering/, 2020e. Accessed: 2020-09-13.
- NVIDIA. Convolutional layers user guide. <https://docs.nvidia.com/deeplearning/performance/dl-performance-convolutional/index.html>, 2020f. Accessed: 2020-09-17.
- NVIDIA. Nvidia multi-instance gpu. <https://www.nvidia.com/en-us/technologies/multi-instance-gpu/>, 2020g. Accessed: 2020-09-13.
- NVIDIA. Multi-process service. <https://docs.nvidia.com/deploy/mps/>, 2020h. Accessed: 2020-09-13.
- NVIDIA. Nvidia quadro rtx 6000. <https://www.nvidia.com/en-us/design-visualization/quadro/rtx-6000/>, 2020i. Accessed: 2020-09-17.
- NVIDIA. Matrix multiplication background user guide. <https://docs.nvidia.com/deeplearning/performance/dl-performance-matrix-multiplication/index.html>, 2020j. Accessed: 2020-09-17.
- NVIDIA. Nvidia v100 tensor core gpu. <https://www.nvidia.com/en-us/data-center/v100/>, 2020k. Accessed: 2020-09-17.
- Odena, A. Open questions about generative adversarial networks. *Distill*, 2019.
- OpenAI. Openai five. <https://blog.openai.com/openai-five/>, 2018. Accessed: 2020-09-13.
- Otterness, N. and Anderson, J. H. AMD gpus as an alternative to NVIDIA for supporting real-time workloads. In Völz, M. (ed.), *32nd Euromicro Conference on Real-Time Systems (ECRTS)*, volume 165 of *LIPICs*, pp. 10:1–10:23, 2020.
- Paszke, A., Gross, S., Massa, F., Lerer, A., Bradbury, J., Chanan, G., Killeen, T., Lin, Z., Gimelshein, N., Antiga, L., Desmaison, A., Kopf, A., Yang, E., DeVito, Z., Raison, M., Tejani, A., Chilamkurthy, S., Steiner, B., Fang, L., Bai, J., and Chintala, S. Pytorch: An imperative style, high-performance deep learning library. In *Advances in Neural Information Processing Systems 32 (NIPS)*, pp. 8024–8035. 2019.
- PyTorch. Pytorch examples. <https://github.com/pytorch/examples>, 2020. Accessed: 2020-09-17.
- Qi, C. R. Pointnet: Deep learning on point sets for 3d classification and segmentation. <https://github.com/charlesq34/pointnet>, 2017. Accessed: 2020-09-17.
- Qi, C. R., Su, H., Mo, K., and Guibas, L. Pointnet: Deep learning on point sets for 3d classification and segmentation. *2017 IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, pp. 77–85, 2017.
- Qian, N. On the momentum term in gradient descent learning algorithms. *Neural Netw.*, 12(1):145–151, January 1999.
- Radford, A., Metz, L., and Chintala, S. Unsupervised representation learning with deep convolutional generative adversarial networks. In Bengio, Y. and LeCun, Y. (eds.), *4th International Conference on Learning Representations, (ICLR)*, 2016.
- Rajbhandari, S., Rasley, J., Ruwase, O., and He, Y. Zero: Memory optimizations toward training trillion parameter models. *CoRR*, abs/1910.02054, October 2019.
- Rotem, N., Fix, J., Abdulrasool, S., Deng, S., Dzhabarov, R., Hegeman, J., Levenstein, R., Maher, B., Satish, N., Olesen, J., Park, J., Rakhov, A., and Smelyanskiy, M. Glow: Graph lowering compiler techniques for neural networks. *CoRR*, abs/1805.00907, 2018.
- Sandler, M., Howard, A., Zhu, M., Zhmoginov, A., and Chen, L.-C. Mobilenetv2: Inverted residuals and linear bottlenecks. In *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, June 2018.
- Schaller, R. R. Moore’s law: Past, present, and future. *IEEE Spectr.*, 34(6):52–59, June 1997. doi: 10.1109/6.591665.

- Senior, A., Heigold, G., Ranzato, M., and Yang, K. An empirical study of learning rates in deep neural networks for speech recognition. In *2013 IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 6724–6728, 2013.
- Shallue, C. J., Lee, J., Antognini, J. M., Sohl-Dickstein, J., Frostig, R., and Dahl, G. E. Measuring the effects of data parallelism on neural network training. *J. Mach. Learn. Res.*, 20:112:1–112:49, 2019.
- Strubell, E., Ganesh, A., and McCallum, A. Energy and policy considerations for deep learning in NLP. In *Proceedings of the 57th Conference of the Association for Computational Linguistics (ACL)*, pp. 3645–3650, 2019.
- Sutskever, I., Martens, J., Dahl, G., and Hinton, G. On the importance of initialization and momentum in deep learning. In Dasgupta, S. and McAllester, D. (eds.), *Proceedings of the 30th International Conference on Machine Learning*, volume 28 of *Proceedings of Machine Learning Research*, pp. 1139–1147, Atlanta, Georgia, USA, 17–19 Jun 2013. PMLR.
- Vector Institute. Vector institute for artificial intelligence. <https://vectorinstitute.ai/>, 2021. Accessed: 2021-02-03.
- Turc, I., Chang, M., Lee, K., and Toutanova, K. Well-read students learn better: The impact of student initialization on knowledge distillation. *CoRR*, abs/1908.08962, 2019. URL <http://arxiv.org/abs/1908.08962>.
- Vasilache, N., Zinenko, O., Theodoridis, T., Goyal, P., DeVito, Z., Moses, W. S., Verdoolaege, S., Adams, A., and Cohen, A. Tensor comprehensions: Framework-agnostic high-performance machine learning abstractions. *CoRR*, abs/1802.04730, 2018.
- Vaswani, A., Shazeer, N., Parmar, N., Uszkoreit, J., Jones, L., Gomez, A. N., Kaiser, L. u., and Polosukhin, I. Attention is all you need. In Guyon, I., Luxburg, U. V., Bengio, S., Wallach, H., Fergus, R., Vishwanathan, S., and Garnett, R. (eds.), *Advances in Neural Information Processing Systems*, volume 30. Curran Associates, Inc., 2017.
- Wang, K. A pytorch implementation of mobilenetv3. <https://github.com/kuan-wang/pytorch-mobilenet-v3>, 2019. Accessed: 2020-12-05.
- Wasay, A., Hentschel, B., Liao, Y., Chen, S., and Idreos, S. Mothernets: Rapid deep ensemble learning. In Dhillon, I., Papailiopoulos, D., and Sze, V. (eds.), *Proceedings of Machine Learning and Systems*, volume 2, pp. 199–215, 2020. URL <https://proceedings.mlsys.org/paper/2020/file/3ef815416f775098fe977004015c6193-Paper.pdf>.
- Weights&Biases. Sweeps. <https://docs.wandb.com/sweeps>, 2020. Accessed: 2020-09-17.
- Wu, Y., Schuster, M., Chen, Z., Le, Q. V., Norouzi, M., Macherey, W., Krikun, M., Cao, Y., Gao, Q., Macherey, K., Klingner, J., Shah, A., Johnson, M., Liu, X., Kaiser, L., Gouws, S., Kato, Y., Kudo, T., Kazawa, H., Stevens, K., Kurian, G., Patil, N., Wang, W., Young, C., Smith, J., Riesa, J., Rudnick, A., Vinyals, O., Corrado, G., Hughes, M., and Dean, J. Google’s neural machine translation system: Bridging the gap between human and machine translation. *CoRR*, abs/1609.08144, 2016.
- Xia, F. Pointnet.pytorch. <https://github.com/fxia22/pointnet.pytorch>, 2019. Accessed: 2020-09-17.
- Xie, S., Girshick, R. B., Dollár, P., Tu, Z., and He, K. Aggregated residual transformations for deep neural networks. *2017 IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, pp. 5987–5995, 2017.
- Yi, L., Kim, V. G., Ceylan, D., Shen, I.-C., Yan, M., Su, H., Lu, C., Huang, Q., Sheffer, A., and Guibas, L. A scalable active framework for region annotation in 3d shape collections. *SIGGRAPH Asia*, 2016.
- Yu, F., Zhang, Y., Song, S., Seff, A., and Xiao, J. Lsun: Construction of a large-scale image dataset using deep learning with humans in the loop. *CoRR*, abs/1506.03365, 2015.
- Zajac, Z. hyperband. <https://github.com/zygmuntz/hyperband>, 2017. Accessed: 2020-11-09.
- Zeiler, M. D. ADADELTA: an adaptive learning rate method. *CoRR*, abs/1212.5701, 2012.
- Zhang, Q., Han, Z., Yang, F., Zhang, Y., Liu, Z., Yang, M., and Zhou, L. Retiarri: A deep learning exploratory-training framework. In *14th USENIX Symposium on Operating Systems Design and Implementation (OSDI 20)*, pp. 919–936. USENIX Association, November 2020.
- Zheng, B., Vijaykumar, N., and Pekhimenko, G. Echo: Compiler-based GPU memory footprint reduction for LSTM RNN training. In *47th ACM/IEEE Annual International Symposium on Computer Architecture (ISCA)*, pp. 1089–1102. IEEE, 2020. doi: 10.1109/ISCA45697.2020.00092.
- Zhu, H., Akrouf, M., Zheng, B., Pelegris, A., Jayarajan, A., Phanishayee, A., Schroeder, B., and Pekhimenko, G. Benchmarking and analyzing deep neural network training. In *2018 IEEE International Symposium on Workload Characterization (IISWC)*, pp. 88–100, 2018.

Zhu, H., Phanishayee, A., and Pekhimenko, G. Daydream:
Accurately estimating the efficacy of optimizations for
dnn training. In *USENIX Annual Technical Conference*,
2020.

SUMMARY OF APPENDICES

These appendices cover the following content that does not fit into the paper’s main text due to space constraints.

Appendix A describes the methodology that we use to collect the GPU cluster usage statistics from the Vector Institute. It also provides empirical evidence to support our observation that the dominating single-GPU training jobs often have low hardware utilization.

Appendix B lists the operators that HFTA currently supports as well as their corresponding horizontally-fused counterparts.

Appendix C describes how fused loss functions are handled in order to reconstruct mathematically equivalent gradients.

Appendix D provides empirical evidence that HFTA has no impact on the model’s original convergence.

Appendix E discusses our approach to integrate HFTA with existing hyper-parameter tuning algorithms via HFHT in detail.

Appendix F shows how we collect the GPU hardware performance counters and provides the related references.

Appendix G provides additional statistics and insights that can help clarify our observations and conclusions in Section 5.

Appendix H includes additional evaluation methodology regarding our secondary benchmarks (i.e., ResNet-18, MobileNetV3-Large, Transformer and BERT-Medium), convergence validation, HFHT and partial fusion.

Appendix I shows the additional evaluation results on our secondary benchmarks and partially fused ResNet-18.

A “REAL-WORLD” GPU CLUSTER USAGE STATISTICS

We analyzed the job submissions and execution logs for a two-month period (July 1st to Sept. 1st, 2020) from a large GPU cluster belonging to the Vector Institute, an independent, not-for-profit corporation dedicated to research in the field of artificial intelligence and machine learning (Vector Institute, 2021). The cluster services a variety of DL training workloads from the Vector Institute’s community. The community consists of 501 faculty, postdoc and student researchers who have published 263 conference and journal papers from April 2019 to March 2020, including 61 papers in NeurIPS, ICLR, CVPR and ICML.

The cluster includes 4 GPU partitions, V1a (200 P100 GPUs), V1b (40 T4 GPUs), V2 (480 T4 GPUs) and V3 (240 RTX6000 GPUs), where V3 came online in the last few days of the collection period. V2 was recorded for the

entire period, and the other three partitions were recorded for the last 11 days. V2 is distinguished as the largest partition with the least powerful GPUs. The data contains information on 51338 jobs. The total number of GPU hours spent in these two months amounts to 471768 (equivalent to ~ 317 GPU days per day).

We classify the submitted jobs as “repetitive single-GPU training jobs” if they contain the following submission and execution patterns:

1. Each job only requests a single GPU despite the availability of multiple GPUs on the same node (i.e., not single-node distributed training). The job also does not require specifically which node the GPU resides (i.e., not multi-node distributed training). Therefore, it can only be a single-GPU training job.
2. Within a short time period (60 seconds), a batch of such single-GPU jobs are submitted from the same user, which means that the submission of these jobs is automated, and possibly contains the same code/program with varying parameters.⁷
3. The job names are very similar within the batch for such a short time period. We determine the similarity by calculating the normalized Levenshtein distance (Levenshtein, 1966) among job names with a threshold of 0.9. As a reference, the distance score between two job names ranges from 0 to 1, where 1 represents being completely identical and 0 represents being different. This filter further verifies that these jobs are repetitive single-GPU jobs since the job names are very similar. Afterwards, a manual inspection of the job names within the batches indicates that those names usually contain small variations such as learning rate value or optimizer choices and settings.

We further reached out to individual users to confirm our conclusion. We interviewed 11 active (i.e., most frequent) users of the GPU cluster: (1) 7 users responded that more than 50% of their jobs are repetitive single-GPU training for purposes including hyper-parameter tuning; and (2) 4 of those 7 users submitted over 95% of their jobs for repetitive single-GPU training. The GPU hour usage distribution is plotted in Figure 9.

Since the cluster does not actively monitor GPU hardware performance counters, we randomly sampled several jobs tagged as repetitive single-GPU training jobs and manually gathered the performance counters. Based on the `sm_active` and `sm_occupancy` (explained in Section 4 and elaborated in Appendix F) metrics from our samples, we

⁷The exact code for each job was not available to us due to security/IP concerns.

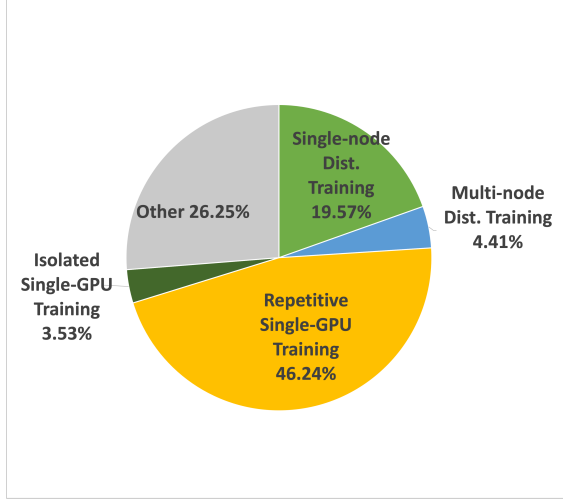


Figure 9. GPU hour usage breakdown for two consecutive months of a large GPU cluster from the Vector Institute.

observe that many of the repetitive single-GPU training jobs can severely under-utilize the GPUs both temporally and spatially (as shown in Figure 10a and Figure 10b, respectively). The maximum `sm_active` among the sampled jobs is 24%, and maximum `sm_occupancy` is 14%.

B HFTA OPERATOR FUSION RULES

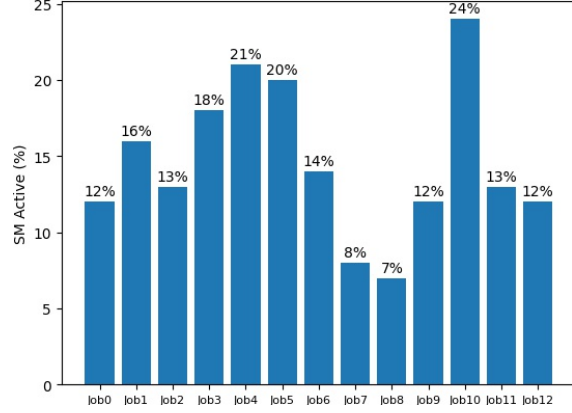
We list the horizontal operator fusion rules for 17 PyTorch operators in Table 6. The left column contains the original operators, and the right column indicates using which operator we could get the mathematically equivalent horizontally-fused version of B original operators. These operators are commonly used in DL research and development, and sufficient to implement a wide range of state-of-the-art DL models. Building on top of these fusion rules, we further develop the fused multihead attention layer and the fused Transformer encoder layer to support models that are based on the attention mechanisms or transformers.

C FUSED LOSS

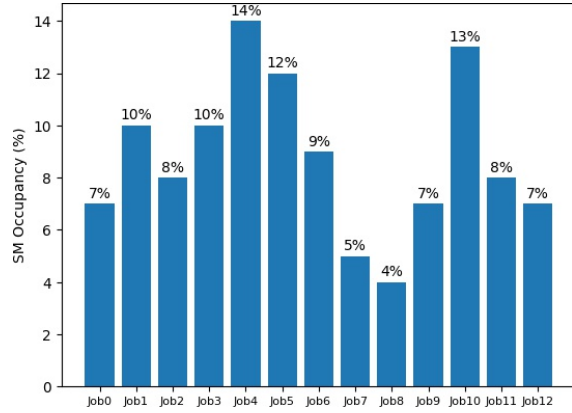
In the following, we show how loss fusion is handled in order to reconstruct mathematically equivalent gradients. The inter-model horizontally fused loss with *mean reduction* is shown as:

$$\mathcal{L} = \frac{1}{B} \sum_{b=0}^B \ell_b \quad (1)$$

where ℓ_b is the loss of the b -th model, and there are B models in total contributing to the fused loss \mathcal{L} . Taking the gradients on both side of Equation 1 with respect to the parameters $\vec{\theta}_\beta$ of a specific model β results in:



(a) `sm_active`



(b) `sm_occupancy`

Figure 10. GPU hardware performance counters measured via DCGM (Kukanur, 2016) for 13 jobs sampled from the clump of repetitive single-GPU training jobs.

$$\nabla_{\vec{\theta}_\beta} \mathcal{L} = \frac{1}{B} \nabla_{\vec{\theta}_\beta} \sum_{b=0}^B \ell_b = \frac{1}{B} \sum_{b=0}^B \nabla_{\vec{\theta}_\beta} \ell_b = \frac{1}{B} \nabla_{\vec{\theta}_\beta} \ell_\beta \quad (2)$$

because $\nabla_{\vec{\theta}_\beta} \ell_b = 0$ if $b \neq \beta$. We can rearrange Equation 2 into:

$$\nabla_{\vec{\theta}_\beta} \ell_\beta = B \nabla_{\vec{\theta}_\beta} \mathcal{L} = \nabla_{\vec{\theta}_\beta} B \mathcal{L} \quad (3)$$

We can recognize that the expression on the left-hand side of Equation 3 is precisely the gradients for model β if each model were trained independently. Therefore, in order to reconstruct exactly the same gradients when training via HFTA, the final fused loss \mathcal{L} needs to be scaled by B . Similarly for the fused loss with *sum reduction*:

$$\mathcal{L} = \sum_{b=0}^B \ell_b \quad (4)$$

we can derive that such scaling is no longer needed:

$$\nabla_{\vec{\theta}_\beta} \mathcal{L} = \nabla_{\vec{\theta}_\beta} \sum_{b=0}^B \ell_b = \sum_{b=0}^B \nabla_{\vec{\theta}_\beta} \ell_b = \nabla_{\vec{\theta}_\beta} \ell_\beta \quad (5)$$

Table 6. The horizontal fusion rules for the operators that HFTA currently supports. ‘‘ConvT’’ stands for ‘‘ConvTranspose’’ (a.k.a., deconvolution). \vec{x} , \vec{y} , \vec{w} and \vec{b} represent the input, output, weight and bias tensors, respectively. N , C , H , W and L represent the batch sizes, channel sizes, heights, widths, and signal lengths of the tensors used in convolutions, deconvolution, batch-norms, MaxPool2d, and Dropout2d. G represents the numbers of groups used in the convolutions and deconvolution. F represents the feature sizes of the tensors used in linear layers. D represents arbitrary unmodified dimensions in LayerNorm and embedding layers. E represents the dimensions for normalization in LayerNorm. ϵ and ζ represents the number of embedding vectors and the size of each embedding vector for the embedding layer. * represents zero or more arguments whose values are kept the same. B represents the number of operators horizontally fused together via HFTA.

PyTorch Operator (Tensors: Shapes, Other Parameters = Arguments)	HFTA Horizontally Fused Operator (Tensors: Shapes, Other Parameters = Arguments)
Conv2d(\vec{x} : $[N, C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, \vec{w} : $[C_{\vec{y}}, \frac{C_{\vec{x}}}{G}, H_{\vec{w}}, W_{\vec{w}}]$, \vec{b} : $[C_{\vec{y}}]$, $G = g$, *)	Conv2d(\vec{x} : $[N, B \times C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, \vec{w} : $[C_{\vec{y}}, \frac{B \times C_{\vec{x}}}{G}, H_{\vec{w}}, W_{\vec{w}}]$, \vec{b} : $[B \times C_{\vec{y}}]$, $G = B \times g$, *)
Conv1d(\vec{x} : $[N, C_{\vec{x}}, L_{\vec{x}}]$, \vec{w} : $[C_{\vec{y}}, \frac{C_{\vec{x}}}{G}, L_{\vec{w}}]$, \vec{b} : $[C_{\vec{y}}]$, $G = g$, *)	Conv1d(\vec{x} : $[N, B \times C_{\vec{x}}, L_{\vec{x}}]$, \vec{w} : $[C_{\vec{y}}, \frac{B \times C_{\vec{x}}}{G}, L_{\vec{w}}]$, \vec{b} : $[B \times C_{\vec{y}}]$, $G = B \times g$, *)
ConvT2d(\vec{x} : $[N, C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, \vec{w} : $[C_{\vec{y}}, \frac{C_{\vec{x}}}{G}, H_{\vec{w}}, W_{\vec{w}}]$, \vec{b} : $[C_{\vec{y}}]$, $G = g$, *)	ConvT2d(\vec{x} : $[N, B \times C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, \vec{w} : $[C_{\vec{y}}, \frac{B \times C_{\vec{x}}}{G}, H_{\vec{w}}, W_{\vec{w}}]$, \vec{b} : $[B \times C_{\vec{y}}]$, $G = B \times g$, *)
Linear(\vec{x} : $[N, F_{\vec{x}}]$, \vec{w} : $[F_{\vec{x}}, F_{\vec{y}}]$, \vec{b} : $[F_{\vec{y}}]$)	baddbmm(\vec{b} : $[B, 1, F_{\vec{y}}]$, \vec{x} : $[B, N, F_{\vec{x}}]$, \vec{w} : $[B, F_{\vec{x}}, F_{\vec{y}}]$)
BatchNorm1d(\vec{x} : $[N, C_{\vec{x}}]$ or $[N, C_{\vec{x}}, L_{\vec{x}}]$, \vec{w} : $[C_{\vec{x}}]$, \vec{b} : $[C_{\vec{x}}]$, *)	BatchNorm1d(\vec{x} : $[N, B, C_{\vec{x}}]$ or $[N, B \times C_{\vec{x}}, L_{\vec{x}}]$, \vec{w} : $[B \times C_{\vec{x}}]$, \vec{b} : $[B \times C_{\vec{x}}]$, *)
BatchNorm2d(\vec{x} : $[N, C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, \vec{w} : $[C_{\vec{x}}]$, \vec{b} : $[C_{\vec{x}}]$, *)	BatchNorm2d(\vec{x} : $[N, B \times C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, \vec{w} : $[B \times C_{\vec{x}}]$, \vec{b} : $[B \times C_{\vec{x}}]$, *)
LayerNorm(\vec{x} : $[N, D_1, \dots, D_m, E_1, \dots, E_n]$, \vec{w} : $[E_1, \dots, E_n]$, \vec{b} : $[E_1, \dots, E_n]$, *)	(LayerNorm(\vec{x} : $[B, N, D_1, \dots, D_m, E_1, \dots, E_n]$, \vec{w} : $[E_1, \dots, E_n]$, \vec{b} : $[E_1, \dots, E_n]$) $\times \vec{w} + \vec{b}$); \vec{w}, \vec{b} : $[B, 1, \dots, 1, E_1, \dots, E_n]$
Embedding(\vec{x} : $[D_1, \dots, D_m]$, \vec{w} : $[\epsilon, \zeta]$)	Embedding(\vec{x} : $[B, D_1, \dots, D_m]$ + $(\epsilon, 2\epsilon, \dots, B\epsilon)$: $[B, 1, \dots, 1, m]$, \vec{w} : $[B \times \epsilon, \zeta]$)
MaxPool2d(\vec{x} : $[N, C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, *)	MaxPool2d(\vec{x} : $[N, B \times C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, *)
AdaptiveAvgPool2d(\vec{x} : $[N, C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, *)	AdaptiveAvgPool2d(\vec{x} : $[N, B \times C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, *)
Dropout2d(\vec{x} : $[N, C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, *)	Dropout2d(\vec{x} : $[N, B \times C_{\vec{x}}, H_{\vec{x}}, W_{\vec{x}}]$, *)
Dropout(\vec{x} : $[*]$)	Dropout(\vec{x} : $[*, B, *]$, *)
LeakyReLU(x : $[*]$, *)	LeakyReLU(x : $[*, B, *]$, *)
ReLU(x : $[*]$, *)	ReLU(x : $[*, B, *]$, *)
ReLU6(x : $[*]$, *)	ReLU6(x : $[*, B, *]$, *)
LeakyReLU(x : $[*]$, *)	LeakyReLU(x : $[*, B, *]$, *)
Tanh(x : $[*]$)	Tanh(x : $[*, B, *]$)

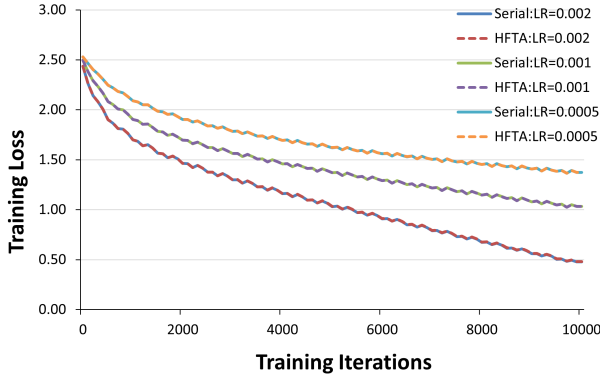


Figure 11. Training loss per iteration when training ResNet-18 on CIFAR-10. LR represents the learning rate. *Serial* represents training each model separately, and *HFTA* represents our method.

In these derivations, no assumption is made on the exact formula of ℓ_{β} , which means such scaling rules are universal to any types of loss functions including regularization.

D CONVERGENCE

Even though HFTA reconstructs the mathematically equivalent gradients for each independently trained model, minor numerical differences can still exist since the order of computations in fused operators can be different from the orig-

inal ones. To demonstrate that such numerical differences do not affect the models’ original convergence empirically, we train a well-known ResNet-18 (He et al., 2016) model on the CIFAR-10 (Krizhevsky, 2009) dataset with three different learning rates.⁸ Figure 11 shows the training-loss-per-iteration curves for training each model independently (solid curves) and collectively as a horizontally fused job via HFTA (dotted curves). Since the dotted curves overlap entirely with the solid ones, we conclude that HFTA-based training maintains exactly the same convergence as independent model training.

E HFHT DESIGN

Many hyper-parameter tuning algorithms and frameworks (e.g., Ray Tune (Liaw et al., 2018)) are built based on the paradigm shown in Algorithm 1: (i) an *algorithm* (e.g., Hyperband (Li et al., 2018)) proposes a batch of sets of hyper-parameters (e.g., H in Algorithm 1) to a job *scheduler* that schedules and runs the evaluations (i.e., the training jobs) of these sets of hyper-parameters; (ii) the algorithm then updates (and hopefully improves) itself using the evaluation results (e.g., R in Algorithm 1, such as validation losses or accuracy) gathered from the output artifacts after those jobs finish. This routine repeats until a certain terminating condition is met while tracking a globally optimal set of hyper-parameters (e.g., \hat{h} in Algorithm 1).

⁸We provide the detailed methodology behind this and other experiments on our secondary benchmarks in Appendix H

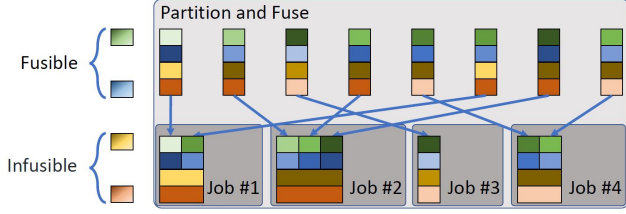


Figure 12. An example showing that the proposed sets of hyper-parameters are partitioned and fused based on their *infusible* hyper-parameters’ values.

Therefore, to integrate HFTA with existing hyper-parameter tuning algorithms, we need to modify the interface between the algorithm and the job scheduler (e.g., line 12 in Algorithm 1). When the algorithm proposes a batch of hyper-parameter sets, we should partition these sets before passing the partitions to the scheduler, and ask the scheduler to run each partition as a fused job (e.g., *partition_and_fuse()* on line 8 in Algorithm 1). When the fused jobs finish, we then scatter/“unfuse” the results into their original orders before sending them back to the algorithm (e.g., *unfuse_and_reorder()* on line 8 in Algorithm 1).

The aforementioned hyper-parameter set partition can be conducted in different ways. In HFHT, we leverage the most straightforward approach. Given a bag of different hyper-parameters, we divide them into two categories: *fusible* and *infusible*. Being fusible means that different values of such hyper-parameters can be co-evaluated in a fused job (e.g., different learning rates or weight initializers), whereas being infusible means that different values of such hyper-parameters can lead to significant difference in the operator types and shapes (e.g., batch size) or change the model architecture completely (e.g., MobileNet V2 vs. V3-Large). Once the users specify which hyper-parameters are fusible and infusible, as we show in Figure 12, HFHT can utilize this information to partition arbitrary sets of hyper-parameter. Afterwards, each partition only has a single value for each infusible hyper-parameter.

To integrate our hardware-based sharing baselines (i.e., *concurrent*, *MPS*, and *MIG*)⁹ with existing hyper-parameter tuning algorithms, since these hardware features treat each job as a separate process, there is no scheduling constraint on the values of the hyper-parameters. Therefore, we simply ask the scheduler to run these jobs as concurrently as the GPU allows.

By default, the tuning algorithms only concern about the impact of each hyper-parameter on the training results’ quality (e.g., accuracy). However, with the introduction of HFTA, each hyper-parameter now is additionally correlated with

⁹These baselines are elaborated in Section 4.

Algorithm 1 Integrating *HFTA*, *concurrent*, *MPS* and *MIG* with a General Hyper-parameter Tuning Routine

```

1:  $\hat{h} \leftarrow \text{NUL}$  {The best set of hyper-parameters.}
2:  $\hat{r} \leftarrow \text{NUL}$  {The best training result.}
3:  $H \leftarrow \emptyset$  {A batch of arbitrary sets of hyper-parameters.}
4:  $R \leftarrow \emptyset$  {Training results corresponding to  $H$ .}
5: while terminating condition do
6:    $H \leftarrow \text{algorithm.propose}()$ 
7:   if HFTA enabled then
8:      $R \leftarrow \text{unfuse\_and\_reorder}(\text{scheduler.schedule\_and\_run}(\text{partition\_and\_fuse}(H)))$ 
9:   else if concurrent or MPS or MIG enabled then
10:     $R \leftarrow \text{scheduler.schedule\_and\_run\_in\_parallel}(H)$ 
11:   else
12:     $R \leftarrow \text{scheduler.schedule\_and\_run}(H)$ 
13:   end if
14:    $\hat{r}, \hat{h} \leftarrow \text{select\_best}((R, H), (\hat{r}, \hat{h}))$ 
15:    $\text{algorithm.update}(H, R)$ 
16: end while
    
```

Table 7. DCGM Metric Names, Field Identifier Macros and IDs

Name	Field Identifier Macro	ID
sm_active	DCGM_FL_PROF_SM_ACTIVE	1002
sm_occupancy	DCGM_FL_PROF_SM_OCCUPANCY	1003
tensor_active	DCGM_FL_PROF_PIPE_TENSOR_ACTIVE	1004
GPU Utilization	DCGM_FL_DEV_GPU_UTIL	203

the hardware utilization of the underlying tuning jobs in terms of how well the fusion opportunities are exposed. Thus, for a specific iteration during tuning, if the algorithm either (1) only proposes a single set of hyper-parameters, or (2) proposes sets that don’t share any common value for the infusible hyper-parameters, there would be few opportunities for HFTA to exploit. In other words, *the exact design of the tuning algorithm itself can be either HFTA-“friendly” or “unfriendly”*. For example, as we show in Section 5.4, random search is a more HFTA-“friendly” algorithm than Hyperband. Therefore, as one direction for our future work, we will investigate how to adjust existing tuning algorithms to extract the most benefits offered by HFTA.

F DCGM METRICS

The `sm_active`, `sm_occupancy` and `tensor_active` performance counters are measured through DCGM (Kukanur, 2016). Their field identifier macros and IDs are listed in Table 7. Please refer to the DCGM Library API Reference Manual (NVIDIA, 2020d) for their precise definitions.

Table 8. The peak training throughput speedups of HFTA over the baselines.

Benchmark		PointNet Cls.	PointNet Seg.	DCGAN	
V100	FP32	serial	2.62	1.62	4.18
		concurrent	2.54	1.62	1.95
		MPS	2.36	1.17	1.95
	AMP	serial	5.02	4.29	4.59
		concurrent	5.02	4.24	2.01
		MPS	4.50	3.03	2.03
RTX 6000	FP32	serial	2.46	1.97	6.69
		concurrent	2.46	1.95	1.64
		MPS	2.07	1.22	1.69
	AMP	serial	4.36	3.63	6.29
		concurrent	4.26	3.54	1.72
		MPS	3.79	2.54	1.82
A100	FP32	serial	5.47	4.56	4.46
		concurrent	5.47	4.56	1.39
		MPS	2.05	1.31	1.37
	MIG	serial	2.10	1.35	1.59
		concurrent	11.50	9.48	3.61
		MPS	12.98	10.26	1.06
AMP	MPS	4.72	2.93	1.09	
	MIG	4.88	3.02	1.09	

Table 9. The maximum training throughput speedups of HFTA over the baselines given the same number of models sharing one GPU.

Benchmark		PointNet Cls.	PointNet Seg.	DCGAN		
V100	FP32	concurrent	1.77	1.62	1.91	
		MPS	1.65	1.17	1.95	
		AMP	3.41	3.12	2.27	
	AMP	MPS	3.05	2.23	2.23	
		FP32	concurrent	2.32	1.95	1.96
		MPS	1.92	1.22	1.78	
RTX 6000	AMP	concurrent	4.14	3.21	1.73	
		MPS	3.75	2.35	1.90	
		FP32	concurrent	4.91	3.97	8.94
	FP32	MPS	1.64	1.04	9.41	
		MIG	1.51	1.07	1.51	
		AMP	concurrent	9.16	7.86	9.07
MPS	3.18		2.13	7.48		
MIG	2.07		1.58	1.20		

G ADDITIONAL EVALUATION STATISTICS

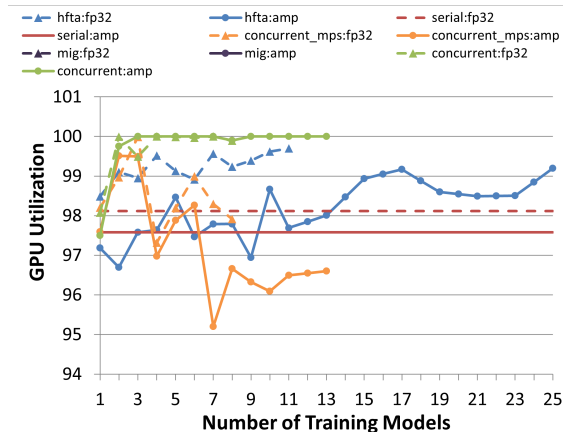
To facilitate the reading of the results from our GPU experiments in Figure 4, we summarize the comparison from different angles between HFTA and the baselines into three tables.

Table 8 shows the peak training throughput comparison between HFTA and the baselines. It is important to highlight that, for both *MPS* and *concurrent*, the training throughput could decrease as we increase the number of models sharing the same GPU (due to host resource contention). Therefore, the “peak” is determined by the highest possible throughput instead of the largest number of models that the GPU can fit (which might or might not lead to the highest throughput). Unlike Table 5, the results here are split between FP32 and AMP to demonstrate how well HFTA performs for each training type.

Table 9 shows the maximum training throughput speedups

Table 10. The maximum speedups of AMP training over FP32.

Benchmark		PointNet Classification	PointNet Segmentation	DCGAN
V100	<i>serial</i>	1.00	1.00	1.00
	<i>concurrent</i>	0.97	1.01	1.07
	<i>MPS</i>	1.01	1.03	1.06
	HFTA	1.92	2.65	1.10
RTX6000	<i>serial</i>	1.06	1.19	1.16
	<i>concurrent</i>	1.09	1.22	1.05
	<i>MPS</i>	1.03	1.05	1.02
	HFTA	1.88	2.20	1.09
A100	<i>serial</i>	1.13	1.13	1.01
	<i>concurrent</i>	1.00	1.05	1.08
	<i>MPS</i>	1.03	1.06	1.03
	<i>MIG</i>	1.02	1.05	1.20
	HFTA	2.37	2.36	0.82


 Figure 13. `nvidia-smi`-defined “GPU utilization” for PointNet classification task on A100.

of HFTA over the baselines, given the same number of models sharing the same GPU. The maximum is picked by varying the number of models sharing the same GPU and finding the largest performance gap between HFTA and the baselines. This helps to isolate the benefits of better SMs and TCs utilization from the benefits of better memory utilization when training via HFTA.

Table 10 shows the maximum training throughput speedups of AMP over FP32 for both HFTA and the baselines. The maximum here is also picked by varying the number of models (except for *serial*, which always only runs one model per GPU) and finding the largest performance gap between FP32 and AMP. This helps to demonstrate that HFTA is more efficient in utilizing advanced hardware compute units such as TCs.

Similar to Figure 7a, 7b and 7c, Figure 13 plots the `nvidia-smi`-defined “GPU utilization” (NVIDIA, 2016) for PointNet classification task training on the A100 GPU. Contrary to a popular belief (Elangovan, 2020; fastai, 2020), we observe that the `nvidia-smi`-defined “GPU utilization” can be sometimes a weak utilization indicator, since

the curves in Figure 13 appear rather noisy and do not follow the trends of throughput improvements in Figures 4g or any hardware counters’ trend in Figure 7a, 7b or 7c.

Similar to Figure 7, Figure 14 plots the `sm_active`, `sm_occupancy`, and `tensor_active` of HFTA and the baselines as we increase the number of models sharing the same V100 GPU. In addition to the observations we already present in Section 5.3, we also observe that the *serial* baselines’ hardware utilization is lower on A100 than on V100. Therefore, Figure 14 provides empirical evidence to support our argument in Section 2.1 and Section 5.1 that newer GPU generations suffer more significantly from the hardware under-utilization of repetitive single-accelerator training workloads.

H ADDITIONAL METHODOLOGY DETAILS

H.1 Secondary Benchmarks

To evaluate the HFTA’s general effectiveness in extracting hardware utilization for conventional models, we further include the following models and tasks as our secondary benchmarks.

ResNet (He et al., 2016) and *MobileNet* (Howard et al., 2017; Sandler et al., 2018; Howard et al., 2019) are two classes of convolutional neural networks that are generally used (or as backbones) in computer vision (CV) tasks. Both classes contain many variants of the models. As our benchmarks, we train ResNet-18 and MobileNetV3-Large (Howard et al., 2019) to perform image classification tasks, though HFTA can be applied on the other variants and tasks as well. We leverage an implementation of ResNet-18 from PyTorch’s official examples (PyTorch, 2020), and an open-sourced PyTorch re-implementation (Wang, 2019) of MobileNetV3-Large. Both models are trained on the CIFAR-10 (Krizhevsky, 2009) dataset. To evaluate HFTA with different training configurations, ResNet-18 is trained using the Adadelta (Zeiler, 2012) optimizer with a batch size of 128, whereas MobileNetV3-Large is trained using the Adam (Kingma & Ba, 2015) optimizer with a batch size of 1024.

Transformer (Vaswani et al., 2017) and *BERT* (Devlin et al., 2019; Turc et al., 2019) are two classes of attention-based language models that are generally used in natural language processing (NLP) tasks. For Transformer, we leverage an implementation from PyTorch’s official examples (PyTorch, 2020) and configure our variant to have 2 encoder layers with 2 attention heads and the hidden size of 128 (similar to BERT-Tiny (Turc et al., 2019) in the parameter size). We train our Transformer variant for the language modeling (LM) task. For BERT, we leverage an open-sourced PyTorch re-implementation (Kim, 2018) and select the BERT-Medium (Turc et al., 2019) variant to perform the masked

Table 11. The algorithm settings for all four end-to-end hyper-parameter tuning workloads. A *set* refers to a set of hyper-parameters. An *epoch* refers to an epoch of training (i.e., the training loop iterates through the entire dataset once). A *round* refers to a single round of successive halving (Jamieson & Talwalkar, 2016) within Hyperband.

Algorithm	Algorithm Settings	PointNet	MobileNet
Hyperband	Maximum Epochs Allowed for a Single Set (R)	250	81
	Inverse of the Fraction of Sets Discarded in Each Round (η)	5	3
	Last Rounds to Skip	1	2
Random Search	Total Sets	60	50
	Epochs per Set	25	20

LM task. Both models are trained on the WikiText-2 (Merity et al., 2017) dataset using the Adadelta optimizer with the batch size and sequence length of 32.

We perform the experiments of all four secondary benchmarks on two ML accelerators: the V100 GPU and TPU v3. We list the detailed specifications of our experimental setup in Table 4. We provide the corresponding evaluation results in Appendix I.

H.2 Convergence

To empirically prove that HFTA does not affect convergence, using three different learning rates (0.0005, 0.001, 0.002), we train ResNet-18 on V100 with the CIFAR-10 dataset using the Adadelta optimizer with a batch size of 1000. The corresponding validation results are provided in Appendix D.

H.3 HFHT

To demonstrate that HFTA can significantly improve the hardware utilization for existing hyper-parameter tuning algorithms via HFHT, we construct the following four end-to-end hyper-parameter tuning workloads: for each of the PointNet and MobileNet classification tasks, we tune eight different hyper-parameters using each of the Hyperband (Li et al., 2018) and random search (Bergstra & Bengio, 2012) algorithms. We leverage an open-sourced implementation of the Hyperband algorithm (Zajac, 2017) and adopt it into HFHT, and we implement the random search algorithm from scratch. We evaluate HFHT across different algorithm settings listed in Table 11, and we list the hyper-parameters that we tune for each task in Table 12. We provide the corresponding evaluation results in Section 5.4.

H.4 Partial Fusion

Even when there are slight differences in the architectures or the operator types/shapes among the models in repet-

Horizontally Fused Training Array: An Effective Hardware Utilization Squeezer for Training Novel Deep Learning Models

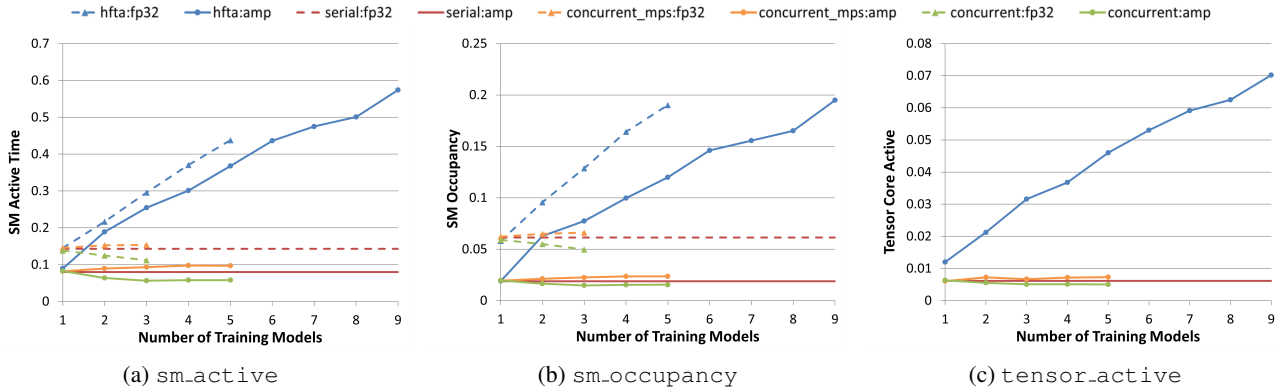


Figure 14. The hardware performance counters for PointNet classification task as we increase the number of models sharing the same V100.

Table 12. The list of hyper-parameters that are tuned for the PointNet and MobileNet classification tasks. “[]” represents a continuous closed interval, whereas “{ }” represents a discrete set.

Hyper-parameter	Fusible	Range	Task(s)
Learning Rate	Yes	[0.0001, 0.01]	Both
Adam’s β_1	Yes	[0.001, 0.999]	Both
Adam’s β_2	Yes	[0.001, 0.999]	Both
Weight Decay	Yes	[0.0, 0.5]	Both
Factor of Learning Rate Decay	Yes	[0.1, 0.9]	Both
Period of Learning Rate Decay	Yes	{5, 10, 20, 40}	Both
Batch Size	No	PointNet: {8, 16, 32} MobileNet: {1024, 2048}	Both
Feature Transformation	No	{True, False}	PointNet
Version	No	{V2, V3-Large}	MobileNet

itive single-accelerator training jobs, HFTA can still improve the overall hardware utilization as long as some parts of the models are horizontally fused. *Model architecture search* (Elsken et al., 2019) and *ensemble learning* (Wasay et al., 2020) can be realistic use cases for such partial fusions. In this section, we want to study the performance sensitivity of the fused model with respect to the extent of the performed fusion.

To conduct such a study, we add *partially fused* optimizers and learning rate schedulers to HFTA, and we extend the ResNet-18 benchmark such that we can individually configure whether each of the 8 basic blocks, the first convolutional block and the last linear block is horizontally fused. We then fix the number of jobs that share the same accelerator (V100) as a constant (30), and measure the per-device training throughput as we incrementally turn *off* the horizontal fusion of each block. We provide the corresponding evaluation results in Appendix I.

I EVALUATION: SECONDARY BENCHMARKS

Similar to Section 5.1 and Section 5.2, to compare HFTA’s end-to-end training performance with our baselines (i.e., *serial*, *concurrent*, and *MPS*) for our secondary benchmarks (i.e., ResNet-18, MobileNet-V3Large, Transformer, and BERT-Medium), Figure 15 and Figure 16 plot the per-device normalized training throughput on the V100 GPUs and the TPU v3 respectively. We normalize the throughput for each experiment by the *serial* (FP32 for V100) baseline. We show both FP32 and AMP training results for the experiments on V100. Each curve grows as we increase the number of models that share the same device. Each curve “stops” when it reaches the maximum number of models before a out-of-memory error occurs, except that the curve for ResNet-18 on TPU stops when the throughput starts to degrade¹⁰.

These figures coincide with the trends in our main observations from Section 5.1 and Section 5.2. Across these secondary benchmarks, on V100, HFTA achieves $2.42\times$ to $3.94\times$ higher peak training throughput over *serial*, $1.67\times$ to $3.02\times$ over *concurrent* and $1.25\times$ to $2.24\times$ over *MPS*; on TPU v3, HFTA achieves $2.98\times$ to $6.43\times$ peak training throughput than *serial*. Therefore, we conclude that HFTA can be also effective in improving the hardware utilization for conventional models during repetitive single-accelerator training.

To evaluate the partial fusion’s performance sensitivity, Figure 17 plots the normalized training throughput when 30 ResNet-18 models share the same V100 GPU as we incrementally turn off the horizontal fusion for each block. We make two observations from this figure. First, a higher de-

¹⁰When we check the TPU usage monitoring dashboard, we observe that the TPU memory usage surpasses its per-core memory capacity when we fuse too many models. Therefore, we hypothesize that the performance degradation could be due to certain memory optimizations (e.g., swapping or rematerialization) employed by the TPU’s memory management system or the XLA compiler.

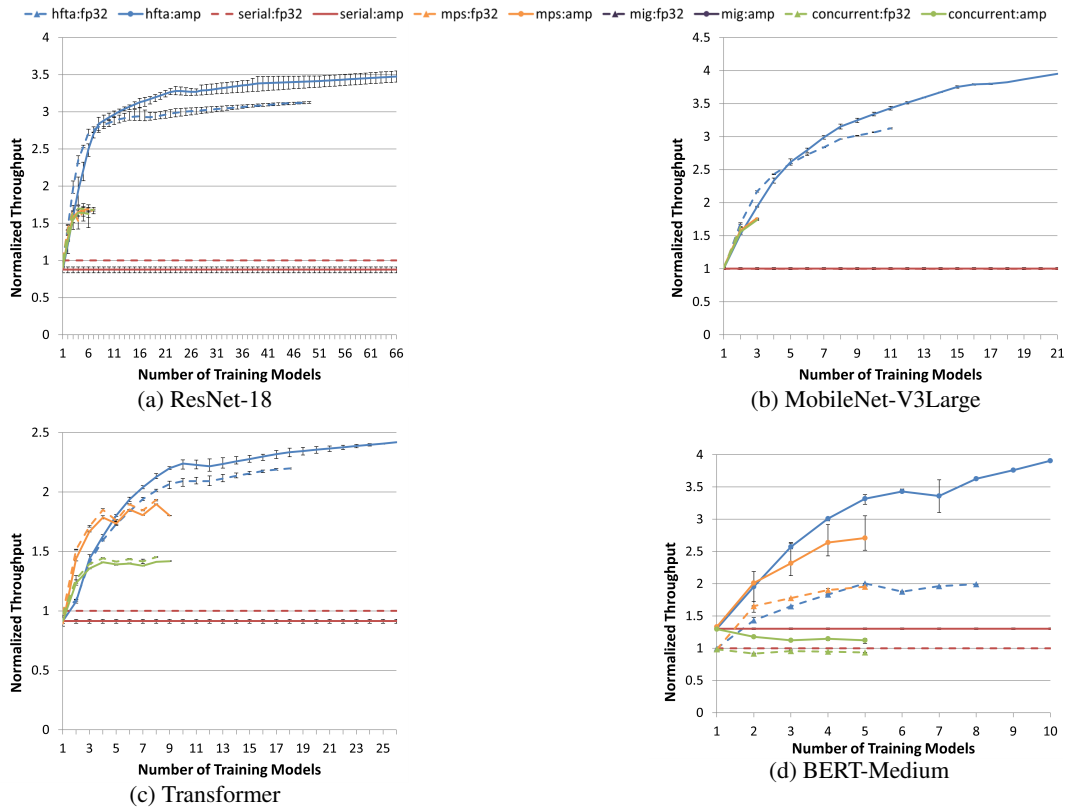


Figure 15. The normalized training throughput as we increase the number of models sharing the same V100 GPU.

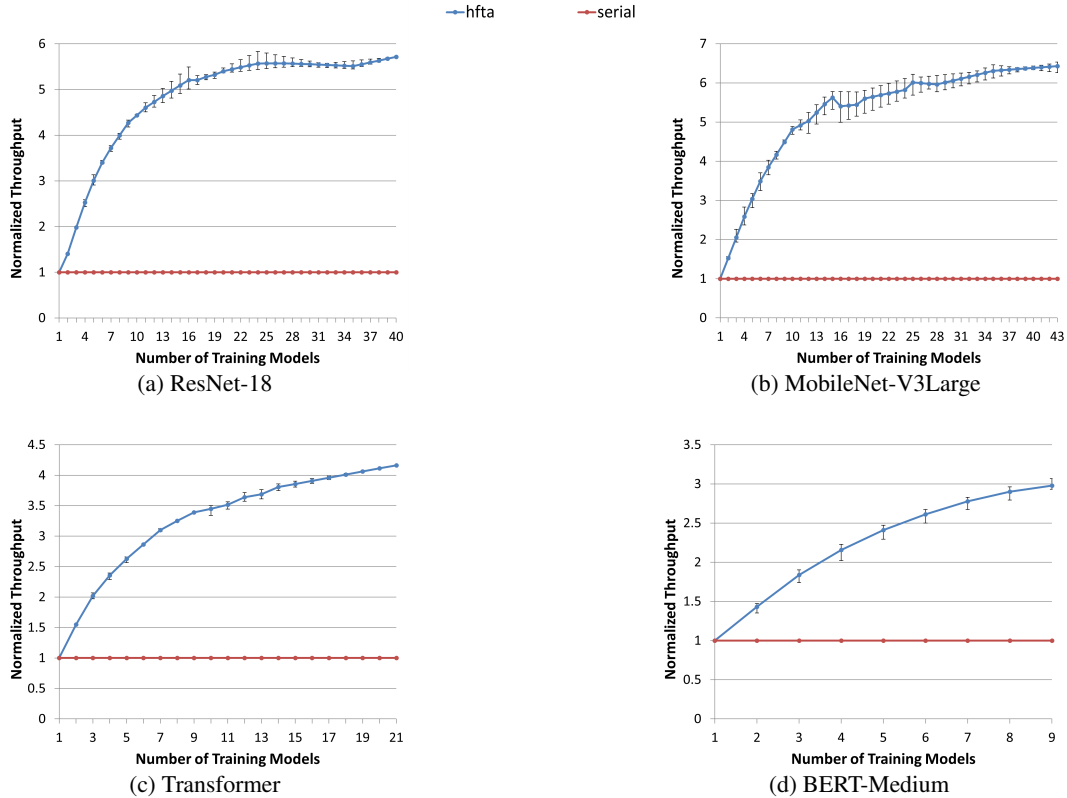


Figure 16. The normalized training throughput as we increase the number of models sharing the same TPU v3 core.

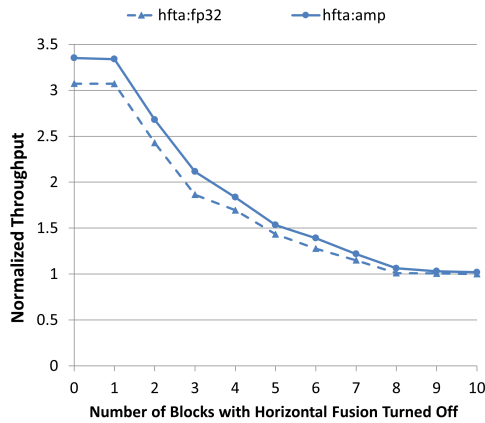


Figure 17. ResNet-18’s normalized training throughput as we incrementally turn off the horizontal fusion for each block.

gree of fusion does lead to better performance. Thus, even if the models among repetitive training jobs can not be fully fused, *every little bit of fusion can still be helpful*. Second, the fusion of different blocks (thus, different operators) contributes differently to the overall performance improvement. This is because some operators within a model suffer more from hardware under-utilization than others.